

# General recommendations for board assembly of Infineon packages

## About this document

### Scope and purpose

This document provides additional information on the board mounting of Infineon packages of SMD and THD types.

### Intended audience

This document addresses all users that are handling the pad and stencil design, the board mounting or the rework of the herein discussed Infineon devices.





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1 Introduction to this document

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This document provides a general overview of handling and board mounting recommendations for Infineon electronic devices. It covers surface mount technology (SMT) as well as through-hole technology (THT) components. The document is the general part of a series of additional information on component board assembly processes. Individual package family-specific board assembly documents provide information that is more detailed. The documents apply in the following order:

- Product specifications (a.g. product application notes or datasheets) overrule package family-specific and general board assembly recommendations
- Package family-specific board assembly recommendations overrule the general document

Throughout this document, the expression “component” refers to a discrete or integrated electronic device that is part of an electronic assembly. Typically, one die or multiple die are enclosed by the component package that features a certain solderable termination type. These terminations (or “terminals”) either can form a distinct lead or can be of a leadless (or “non-lead”) class. Packages with pre-soldered terminations are usually of an array type with melting solder balls (e.g. ball grid array, BGA). Components, which feature multiple die in a distinct package (system-in-package, SiP) are discussed with no specific differentiation from those with a single die. Components, that consist of distinct packages that are pre-mounted e.g. on a laminate substrate (system on a module, SOM) will be referred to as “module packages”.

For package family-specific information of Infineon devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section.

Surface mount technology and surface mount devices

SMT refers to the mounting method used for electronic surface mount devices (SMD). The packages are soldered directly onto the surface of the substrate that features the electronic circuitry. That is typically a printed circuit board (PCB). The type of package terminations depends on the intended application, level of integration, considerations of board level reliability and more. Figure 1 shows examples of Infineon SMD packages.

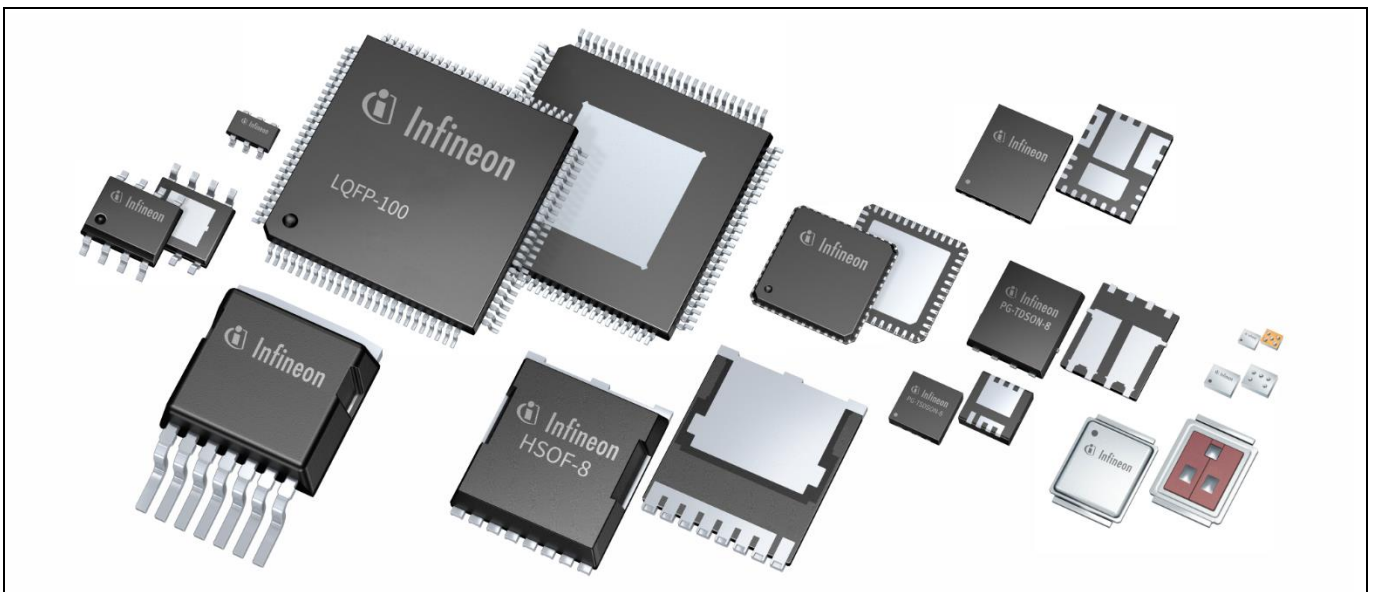
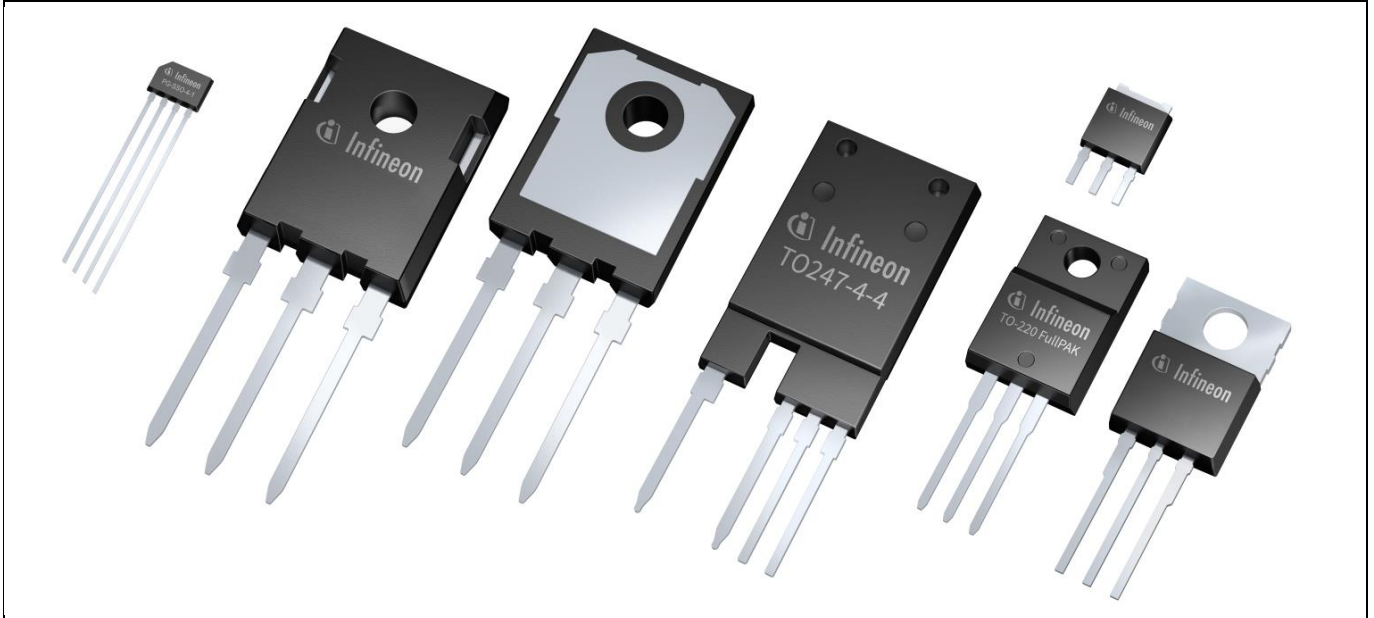


Figure 1 Typical Infineon surface mount devices.

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### Through-hole technology and through-hole devices

THT refers to the mounting method used for electronic through-hole devices (THD). The package pins are inserted into electrically connected plated through-holes of the assembly substrate. They are then soldered to pads on the opposite side. The length and arrangement of such pins depend on the intended application. Some package families, such as transistor outline packages (TO), comprise SMD as well as THD components. [Figure 2](#) shows examples of Infineon THD packages.



**Figure 2** Typical Infineon through-hole devices.

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2 General guidelines

2.1 Packing, transportation and storage conditions

Infineon provides different packings and fixtures depending on devices and customer needs. They comprise e.g. feeding elements for automated pick & place machine (e.g. tape & reel, tray or tube) as well as protective bags and boxes to prevent damage during transportation or storage. The devices are provided either in a non-dry pack or in a dry pack condition. In the latter case, products are packed in an evacuated, sealed moisture barrier bag (MBB) with desiccant and humidity indicator card (HIC) as given in J-STD-033 depending on their moisture-sensitivity level (MSL) [8].

Specific storage conditions such as the storage time of products or product families may be subject to a product specification. In general, the maximum storage duration of the components depends on the specific product and its packing [2][3].

Improper transportation and unsuitable storage of electronic components can lead to a number of issues such as poor solderability or delamination and cracks during subsequent processing. The application guide IEC 61760-2 specifies the transportation and storage conditions for surface mounted devices while the standards series IEC 60721-3-0, IEC 60721-3-1 and IEC 60721-3-2 may be consulted on the classification of environmental parameters and their severities [4][5].

The storage time starts with the date code that is stated on the barcode product label (BPL) that can be found on the outer product packing. Figure 3 shows typical label positions on packing examples. Products shall be processed before the end of the maximum storage time. Processing beyond the expiration date may increase the risk of reduced processing capability, malfunction or even non-function. By reducing contamination sources in the assembly environment (e.g. hazardous gases) risks such as corrosion are significantly reduced.

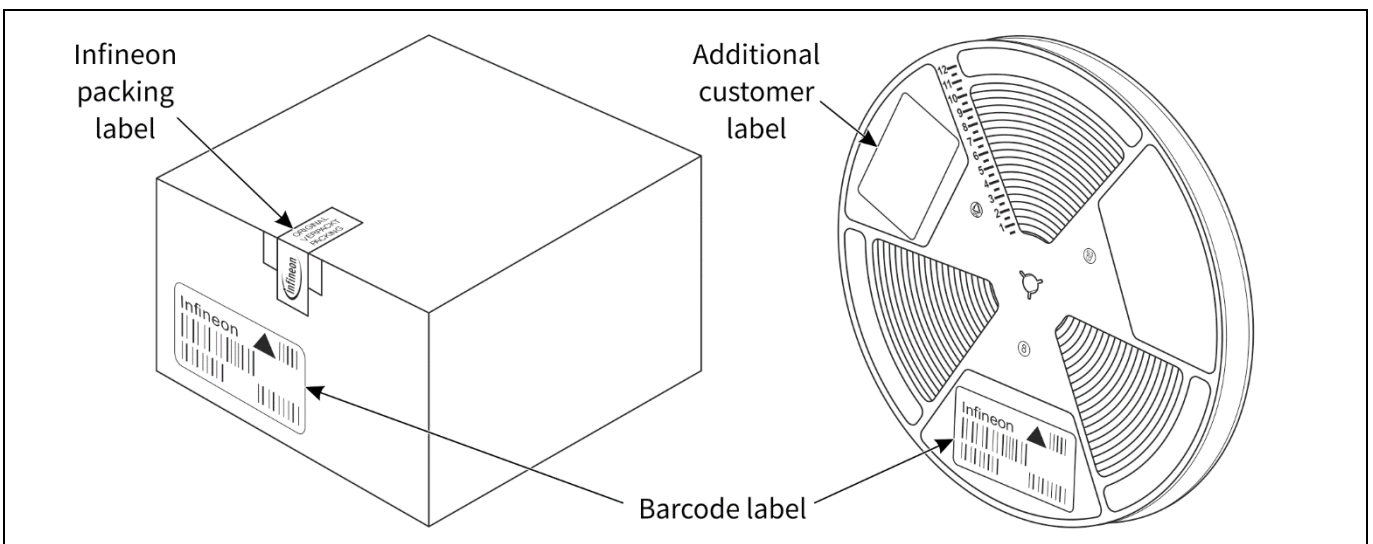


Figure 3 Typical label positions on Infineon packing examples.

For further information about packing, transportation and storage of Infineon devices please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

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2.2 Reflow sensitivity

SMD moisture sensitivity

The package integrity has to be maintained during board mount soldering and de-soldering. Non-hermetic (typically plastic) packages may be moisture-sensitive. Moisture from the ambient air can penetrate into the package mold compound. Increased concentrations of moisture within the package poses the risk for damages due to sudden evaporation during reflow soldering.

Figure 4 shows a typical crack caused by the so-called “popcorn effect”. The crack runs through the mold compound and results in a direct path connecting the lead frame with the package environment. It therefore does not only result in a mechanical weakening of the component but also creates a further site of potential attack by the environment.

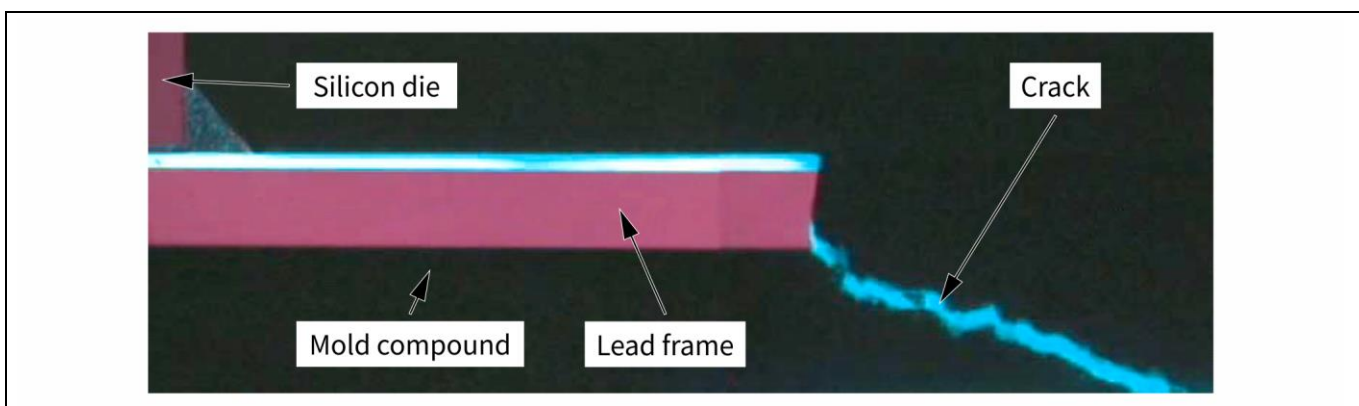


Figure 4 Package crack after reflow shock that is also called “popcorn effect”.

Non-hermetic moisture-sensitive components must be processed in a dry state. They are therefore sealed in moisture-resistant barrier bags and are only removed from their packing immediately prior to their board assembly. The moisture sensitivity level (MSL) specifies the permissible time that a component can remain outside the MBB from opening it until the final soldering process. The J-STD-020 therefore defines eight different MSL classes as shown in Table 1 [7].

Table 1 Moisture sensitivity levels acc. to J-STD-020 depending on the room humidity (RH) [7]

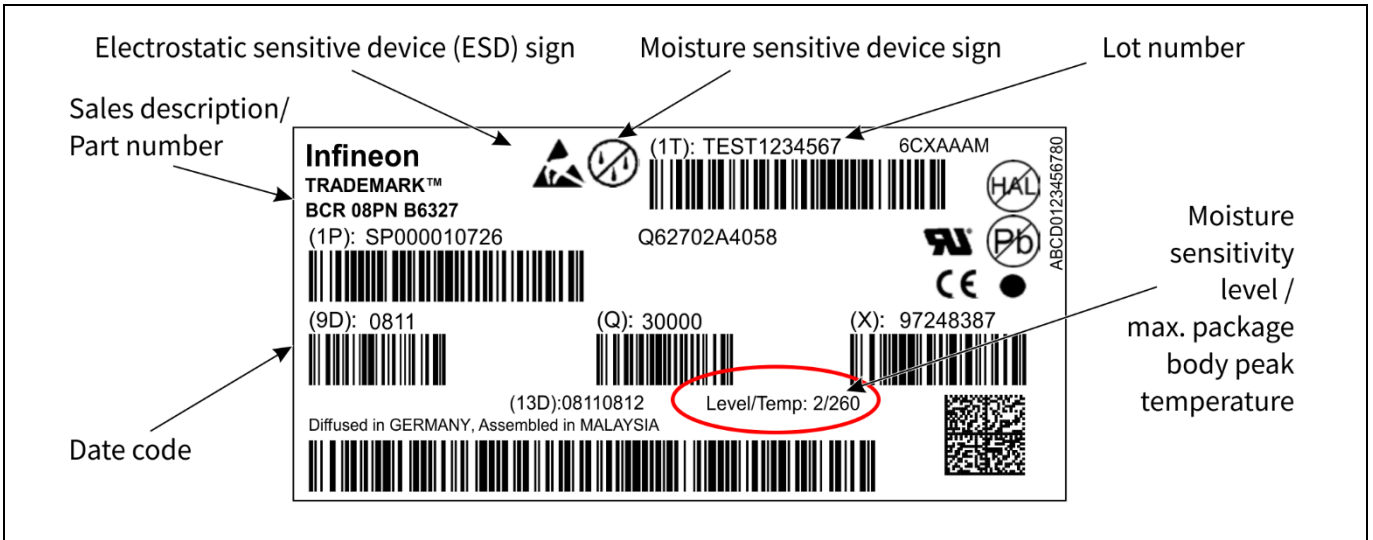
Level	Floor life (out of bag)	
	Time	Condition
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After the bake, board mount reflow must be executed within the time limit as specified on the label.	≤ 30°C / 60% RH

**2 General guidelines**

The MSL classes and package peak temperature are stated on a “moisture sensitivity caution label” on the packing material BPL as shown in Figure 5.

The following items should be considered:

- Storage life (from BPL date code including shelf life) is the time the component is allowed to stay in its proper packing under specific environmental conditions
- Floor life is the time the component is allowed to stay outside its proper packing under specific environmental conditions



**Figure 5 Example of Infineon product barcode label including the moisture sensitivity level / maximum reflow temperature combination.**

The components shall be processed within their maximum floor time. Depending on their MSL classification, they may have to be dried prior to the assembly process as a mandatory step. The J-STD-020 allows a maximum baking condition of up to 125 +5/-0 °C for 24 hours for drying a package [7]. It must be considered, however, that multiple baking runs may cause solderability issues due to oxidation and/or growth of intermetallic phases. It should also be considered, that some packing materials for component feeding like trays, tubes, reels or tapes might not withstand the target baking temperature. For alternative drying conditions of mounted or unmounted SMD packages, please refer to the J-STD-033 [8].

*Note: Baking moisture-sensitive components can reduce the risk of package damage caused by absorbed water during soldering but cannot substitute for proper moisture-resistant packing.*

For further information on drying of Infineon devices, please contact your local sales, application, or quality engineer.

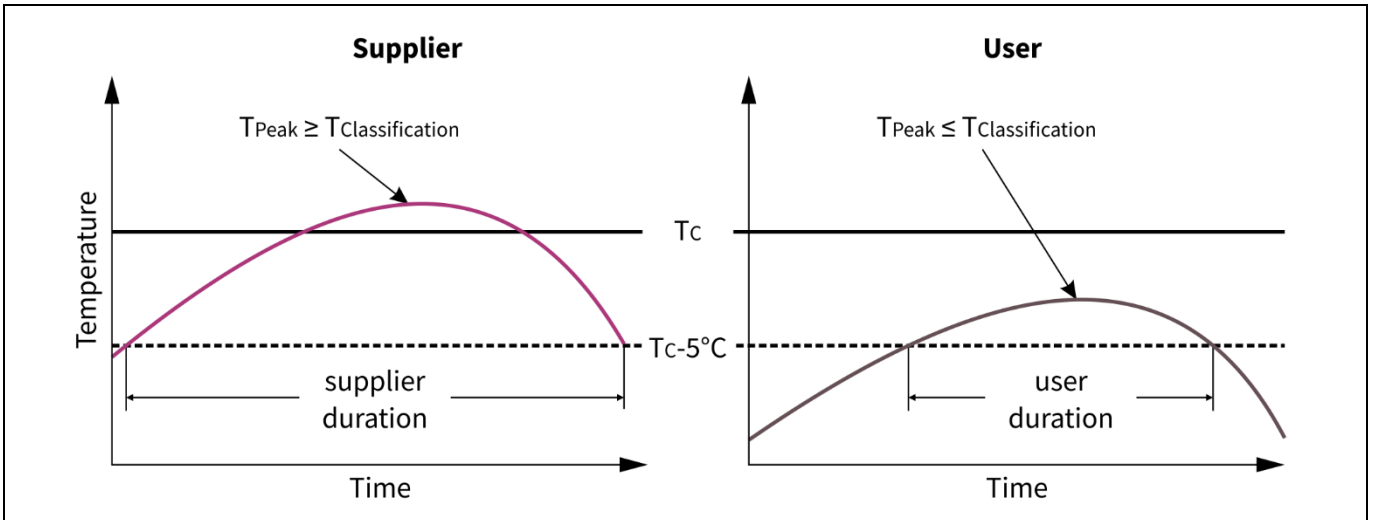
The MSL classification reflow profile according to the J-STD-020 must not be confused with a solder joint reflow profile for component board assembly. The classification reflow profile is measured at the top at the center of the package body surface that is facing up during assembly reflow (also called “live-bug”). It is not measured at the solder joint, where the solder material reflow happens [7]. That is why the corresponding peak temperature is called the “package peak temperature” in contrast to the “reflow peak temperature”. For actual solder reflow profiles, please refer to Section 4.5.

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Figure 6 shows the relation between the supplier qualification and the user application peak temperature according to J-STD-020. The device user must stay below the qualification profile [7].

*Note: The MSL classification reflow profile must not be confused with a solder joint reflow profile for component board assembly. The user must stay below the classification profile.*

Components that are MSL classified by Infineon generally have been tested by three reflow runs in accordance with the J-STD-020 qualification profile. That represents a double-sided reflow and one rework cycle [7].



**Figure 6** Maximum endurable peak temperature at the package body according to J-STD-020. The component supplier qualifies the component with a classification temperature  $T_P$  that is higher than  $T_c$ . A user reflow solder profile peak  $T_P$  must stay below the classification temperature  $T_c$  [7].

**Through-hole mounting**

The heat resistance of wave-solderable THD is tested according to JESD22-B106. That provides the maximum acceptable temperature and time for wave soldering [9].

For further information about moisture sensitivity and product barcode labels of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

**2.3 Termination solderability**

The solderability term generally describes the ability of a plated metal surface to be wetted by molten solder. It refers to how well and uniform the interfacing bond between solder and base metal is made and remains.

The final finish of a package termination ensures its solderability during the specified maximum durations of storage and floor life. The final finishes may be based on plated matte Sn or Ni/Au type stack ups. Ball grid array packages are already pre-soldered when introduced to the board assembly. Improper transportation and unsuitable storage of electronic components may harm the solderability and especially the wetting performance.

Non-plated areas of a package termination are generally excluded from solderability assessment. Such areas do not feature a final finish, which is necessary for proper wetting. An example for such areas are the cut or



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stamped tips of gullwing type terminations. The solderability of Infineon components is qualified according to the standards J-STD-002 or IEC 60068-2-58 [11][12].

The lowest temperatures and durations of the components in the application assembly process shall be measured at their package termination. There, the solder joint formation by material reflow takes place. The user must then stay above this minimum wettability temperatures and durations. For actual solder reflow profiles, please refer to [Section 4.5](#).

For further information about solderability of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

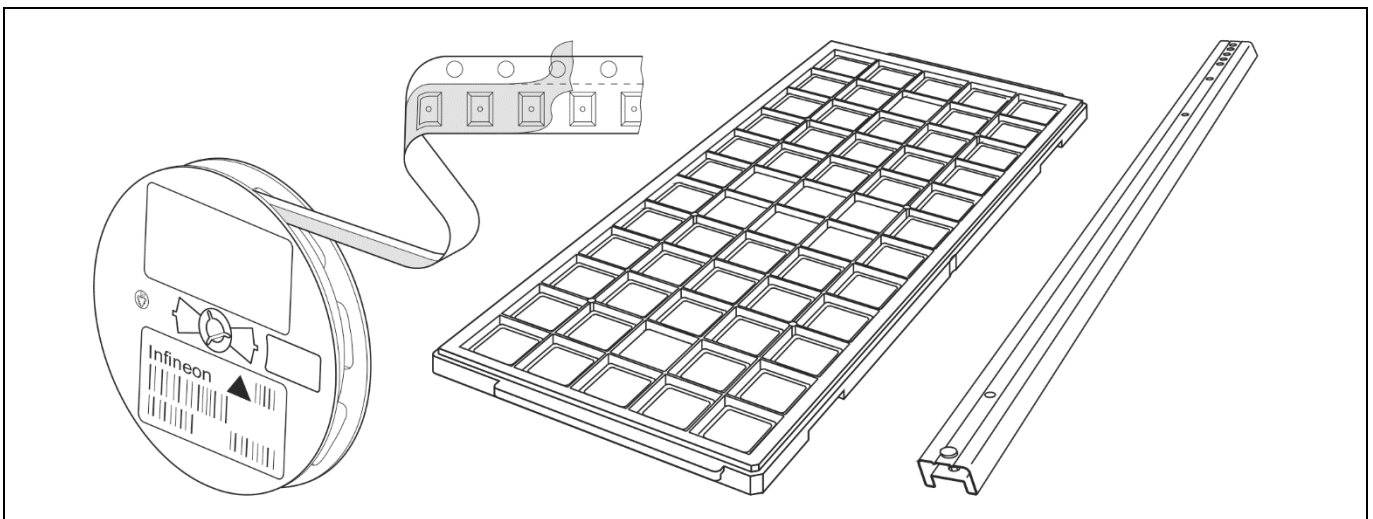
### 2.4 Handling and processing

Different packings and fixtures are available for automated pick & place feeding. Depending on component and customer needs package feeding can happen for example from tape & reel, tray or tube as shown in [Figure 7](#).

Packed Infineon devices are generally ready to use. Manual or improper automated handling of the components may lead to contaminations or cause mechanical damage to their packages or their electrical contacts. Unintentional bending of leads may not only damage the terminations but also the package body with negative consequences to the electrical functionality. Contaminations may lead to solderability issues, corrosion or electrical failures by conductive particles. The standards series IEC 60286 may be consulted for more details on packaging of components for automatic handling [13].

Pre-mount bending and cutting of through-hole components may be needed e.g. to fit the pitch of the solder holes or to mount additional external heat sinks. For further information on THD lead bending and cutting, please refer to [Section 5.2](#).

For further details about specific packing of Infineon devices, please refer to the package database that is available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show a list of available packing solutions for each package.



**Figure 7** Examples of packing for automated feeding: tape and reel, tray, tube.

For further information about automated and manual handling of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

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### 2.5 ESD protective measures

Semiconductor devices are typically sensitive to excessive electrostatic discharge (ESD). They therefore require specific precautionary measures regarding handling and processing. A flow of electrostatic charge through a device can be caused by human touch or by processing tools. The resulting high current and/or high voltage pulses can damage or even destroy sensitive semiconductor structures.

Devices may also be charged when getting in contact with charge source without proper ESD protective measures. Subsequent handling may then result in damages caused by sudden so-called “hard” discharge. A few suggestions on handling and processing are provided below.

#### Equipment for staff

- Dissipative/ conductive footwear or heel straps
- Suitable smocks
- Wrist straps with safety resistors
- Gloves or finger coats which are ESD-proven (with specified volume resistivity)

#### Workplace configuration

- Standard marking of ESD protected areas
- Access controls, with wrist strap and footwear testers
- Air conditioning
- Dissipative and grounded floor, working and storage areas, chairs
- “Ground” potential bonding points for wrist straps
- Trolleys or carts with dissipative surfaces and wheels
- Suitable shipping and storage containers
- Protection against sources of electrostatic fields

#### Production installations and processing tools

- Machine and tool parts made of dissipative or metallic materials
- No materials having thin insulating layers for sliding tracks
- All parts reliably connected to ground potential
- No electric potential difference between individual machine and tool parts
- No sources of electrostatic fields

The standards ANSI/ESD S20.20 and the IEC 61340-5 series provide requirements and guidelines on protection of electronic devices from electrostatic phenomena [14][15].

For further information about ESD conformal handling of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

### 2.6 X-ray radiation

It has been well established that semiconductor components can suffer damage from (dis)charging effects caused by X-ray energy. While this phenomenon does not always result in a hard failure, customers might have no way to recover from the effects of the X-ray exposure.

## 2 General guidelines

X-rays, basically, behave the same as visible light rays, since both are wavelike forms of electromagnetic energy carried by particles called photons. The difference between X-rays and visible light rays is the energy for individual photons (energy is inverse to wavelength).

Infineon studies have shown that there may be a change in the threshold voltage depending on the X-ray dose. This section shows how such damage can be avoided. It also provides typical doses that typically have no impact to the functionality and data retention of semiconductor devices.

### Application of X-ray inspection

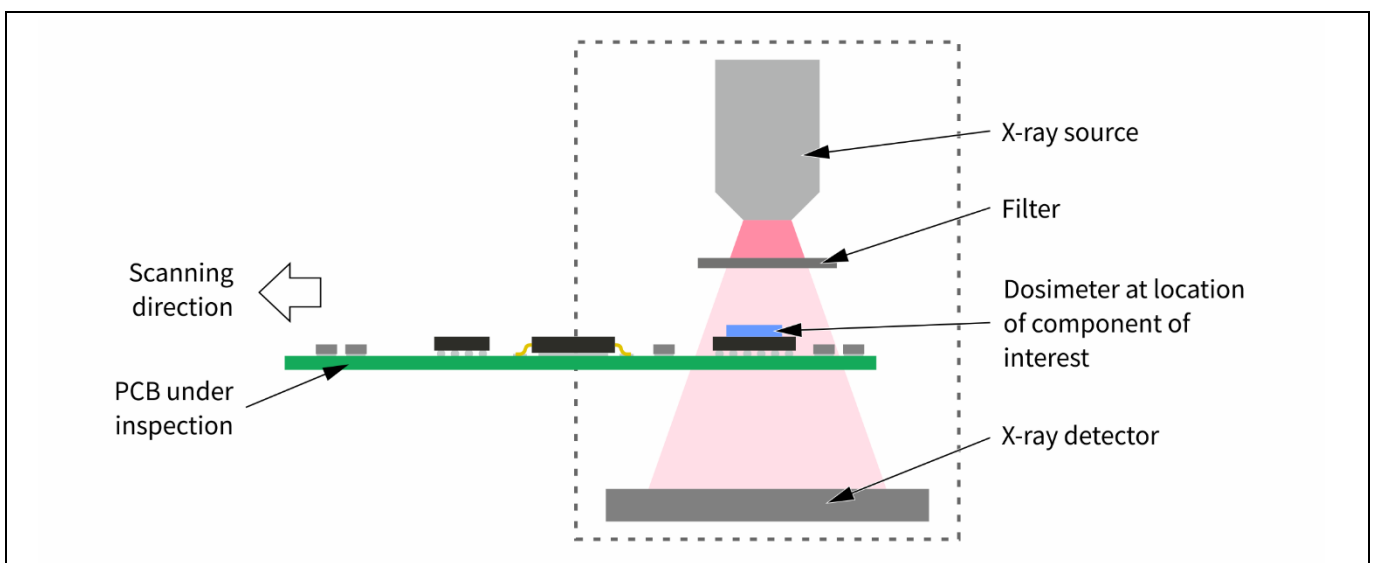
X-ray inspection may be applied for productive inspection (either in-line screening or off-line monitoring) or for failure analysis. For productive components, being delivered to the customer afterwards, the focus should be on lowest energy dose levels while giving the required inspection resolution. However, components under failure analysis will not be delivered to the customer and higher doses can be used to serve the purpose of root cause finding.

X-ray used in security checks before flight transport are not considered here, since they typically apply by orders of magnitude lower energy levels, which are not critical to semiconductor components.

If X-ray inspection is used in productive environment e.g. for incoming packing inspection or automated X-ray inspection (AXI) of assemblies, it is of importance to know the applied energy while keeping it at a minimum. The critical applied energy in this case is the effective cumulative dose that reaches the semiconductor device.

### Measurement of X-ray doses

Typically, information about the dose that reaches the component cannot be taken from the X-ray equipment directly. The only reliable and comparable way to measure the applied energy dose during inspection, is to place a dosimeter at the location of the semiconductor component during the setup of the inspection program as shown in Figure 8. Using this, a correlation of the used equipment, settings, setup, filters and duration to the effective dose at the location of the component can be acquired. For estimation purpose during setup, one can consider that the dose has a linear dependency on the applied tube current and inspection time, an inverse quadratic dependency on the distance between source and component and just a minor dependency on the acceleration voltage.



**Figure 8 Recommended setup to measure the applied energy dose in a reliable and comparable way.**

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### Reduction of X-ray doses in the semiconductor component

In many cases, inspection instruments subject components to X-ray dose values that are significantly higher than what is necessary to achieve reliable inspection results. The key is to minimize the total cumulative dose to the component while achieving a useful inspection image.

There are many commercially available AXI systems and each employs different X-ray set up conditions and exposure doses. It is not possible to provide a single set of recommendations that will apply to all inspection systems. As a rule, customers should limit the cumulative X-ray inspection exposure to the devices to as small a value as possible. Infineon recommends the following mitigation techniques for productive inspection:

- Use the smallest X-ray tube current possible that still produces adequate images.
- Use the largest X-ray tube to sample distance possible that still gives the needed image resolution.
- Use the shortest inspection time possible: fast scan for entire PCB or short shots for dedicated components. Avoid 3D scans wherever possible.
- Use a filter between source and inspected components to reduce the amount of lower energy radiation reaching the semiconductor.
- Inspect from PCB bottom side where possible, so PCB Cu traces and lead frames of components add a filtering effect.

The use of electrical detection techniques such as “boundary scan” may be another strategy to avoid the application of X-ray inspection at all.

### Recommended maximum X-ray dose

In order to obtain good resolution images with modern X-ray equipment, doses in the range of 10-100 mGy (1-10 Rad) should be sufficient. Generally, Infineon recommends not to exceed a cumulative dose of 1 Gy (100 Rad) unless not specified otherwise in the package family-specific board assembly recommendations, product application notes or data sheets.

*Note: Infineon generally recommends not to exceed a cumulative dose of 1 Gy (100 Rad)*

For further information about the inspection by X-ray of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

3 General acceptance criteria of electronic assemblies

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3.1 Solder joint geometry

The quality and reliability of solder joint interconnects for electronic assemblies are influenced by various factors from the used materials, designs and processes. General guidelines on requirements and acceptance of soldered electronic assemblies can be found in IPC-A-610, IPC J-STD-001, or IEC 61191-1 [16][17][18].

Surface mount connections

The solder joint of SMD is located on the same side of the PCB where the component body is located and the solder is applied.

SMD packages provide various types of termination that, from a solder joint geometry point of view, may roughly be divided into leaded, leadless (or non-leaded) and pre-balled ones. Especially the leadless packages may be further sub-divided into lead frame based ones like QFN or laminate-based ones like LGA. Irrespective of their classification, most of the SMD terminations have in common that the solder joint is mainly formed below the package body.

It is generally recommended to target a frustum shaped solder joint geometry having the PCB solder pads slightly larger than the package landing area. Appropriate pad extensions should be applied especially to lead frame packages e.g. for ensuring a proper heel wetting at a gullwing lead but also to leadless packages to enhance the solder joint reliability or self-alignment. Pre-balled BGA type packages are providing the majority of the solder for the final joint by themselves. A joint configuration may be chosen here, that targets a pseudo-ball shape. Figure 9 shows general schematics on typical SMD solder joint configurations.

The distance between the package body bottom side and the PCB pad top side is generally defined as the package “stand-off”. On e.g. gullwing packages the stand-off is dictated by the leads giving the distance of a potential heat sink at the package body to the PCB. Single-side terminated gullwing packages are naturally resulting in a non-symmetric stand-off. Solder balls have a direct impact on the final solder joint height, although it is not matching the initial solder ball diameter. The solder joint height of leadless packages is solely manipulated by the solder volume from board mount print.

Minimum and maximum wetting heights are usually specified depending on quality classes of the electronic assembly. There may also be further subdivisions within one termination geometry group (e.g. toe-down vs. flat gullwing leads in IPC-A-610) that affect the acceptability of the assembly per class. Generally, the solder should not touch the mold body. The tips and edges of terminations that are stamped or sawn are not intended to be solderable by design as they feature bare copper. They therefore have to be excluded from such evaluations as per IPC-A-610 [16].

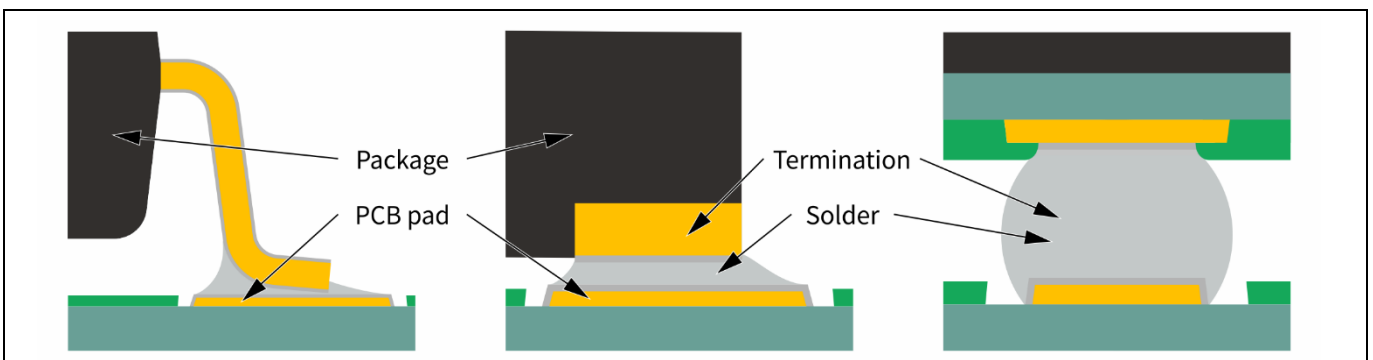
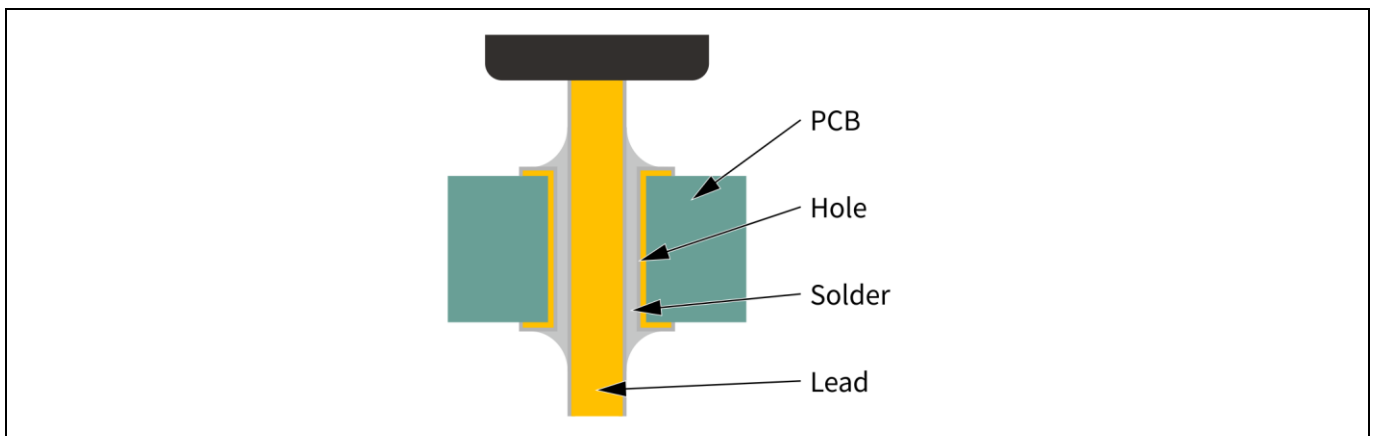


Figure 9 Schematics of SMD solder joint examples with (from left to right) gullwing lead, leadless termination, and solder ball. The depictions are not to scale.

**3 General acceptance criteria of electronic assemblies**

**Through-hole connections**

The solder joint of THD is generally separated into a solder destination side, containing the majority of the component bodies, and a solder source side that gets in contact with the solder wave. The components on the primary solder destination side should not obstruct the solder flow onto the land of the plated through-holes that are part of the joint. The lead should be discernible in the solder, while that also should not get in contact with the mold body. The target solder fill on the secondary solder source side depends on the applied defect condition class as per IPC-A-610. Figure 10 shows a schematic of an ideally wetted THD lead. A non-wetted punched lead tip is not a rejection criterion according to IPC-A-610, as it does not feature a solderable finish [16].



**Figure 10 Schematic of a THD solder joint example.**

For further information about the package-specific board mounting of Infineon devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section. Please also feel free to contact your local sales, application, or quality engineer.

**3.2 PCB pads and through-holes**

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite to each other on either side of a PCB when doing double-sided mounting. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions. The package-board interaction may depend on multiple factors by the PCB. That may be the PCB technology itself or specific board manufacturer design rules.

*Note: Infineon board mounting recommendations are based on generic use cases. The specific PCB technology, design and manufacturing may have a direct impact on their applicability.*

**PCB pad finishes**

The wetting, alloying and therefore the overall solderability of a PCB landing pad depends on its surface finish type and quality. In general, there is no recommendation for a specific combination of PCB pad finish and Infineon device. The quality of the finish in terms of geometry (i.e. flatness) is, however, particularly important for fine-pitch applications. A non-exhaustive selection of typical pad finishes is shown below.

## 3 General acceptance criteria of electronic assemblies

Electroless tin and electroless silver: Solder joints on immersion tin and silver finishes are made directly between the copper of the pad and the solder. The phase growth of the widely used tin-silver-copper solder alloy (SAC) on tin or silver is well understood. The long-term stability of these finishes, especially after baking the PCB (e.g. for drying purposes), may be a concern due to oxidation of the surface or accelerated growth of the intermetallic compound (IMC). The thin layers of  $< 1 \mu\text{m}$  and  $\geq 1 \mu\text{m}$  thickness of Ag and Sn respectively, provide a high flatness that allows for assembly of fine pitch packages.

Electroless nickel (electroless palladium) immersion gold (ENIG/ENEPIG): Electroless Ni/Au finishes provide a stable solderability and very flat surface. The solder joint is made with a 3 to 7  $\mu\text{m}$  thick Ni layer after dissolving the sacrificial Au or Au/Pd layer. Ni-rich IMC from the ternary Cu-Ni-Sn system are forming.

Organic surface preservatives (OSP): Surface protection by organics is done with a sub-micrometer layer that allows for the fabrication of very flat pads. The solder wetting usually occurs only on areas that have been reached by the flux. The coating should be handled carefully to avoid mechanical damage. It is recommended to use an inert reflow atmosphere when manufacturing double-sided assemblies.

Hot-air solder leveling (HAL/HASL): Solder finishes leveled by hot air feature an uneven surface profile with solder humps. Such pad surfaces are therefore less preferred, especially for finer pitches  $< 0.65 \text{ mm}$ . The pre-soldered layers can easily reach thicknesses  $> 5 \mu\text{m}$ . The finish has been widely used in electronics assembly because the method is well known.

Galvanic gold: Galvanic gold finish with its relatively high thickness  $> 1 \mu\text{m}$  especially of hard gold is typically used for connectors. It is not recommended for solder pads due to its low alloying tendency.

### Thermal management

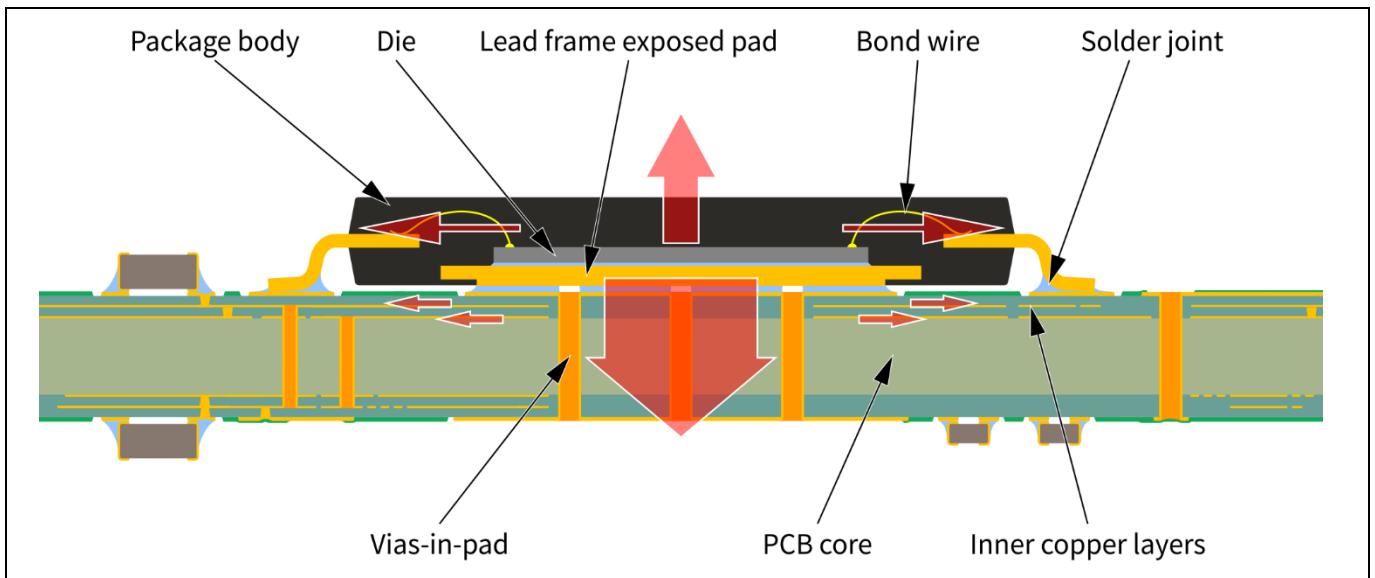
Semiconductor power devices may generate heat that cannot be transferred away sufficiently through the package body. The overall thermal performance of a package in a system is generally characterized by junction-to-ambient thermal resistance chains. Usually the application of the device defines the thermal requirements of the system while the package type and outline provides the boundary conditions for the implementation of the thermal management on the PCB assembly. [Figure 11](#) shows a schematic of thermal management based on the bottom-side cooling (BSC) concept.

Several leaded and leadless packages feature some type of exposed die pad that does not only act as an electrical connection but also forms a heat sink. The thermal performance of a device can be increased by soldering that heat sink to a pad on the PCB. Typically, the heat transfer is supported by plated through holes (PTH) in such a pad acting as thermal vias to the other side of the board. These vias may have an impact on the board design and assembly depending on the specific via type (see [Section 4](#)).

*Note: The connection of a SMD exposed die pad to the board requires reflow soldering. Wave soldering is usually not applicable.*

Alternative concepts to bottom-side cooling are provided by top-side cooling (TSC) and double-side cooling (DSC). TSC allows decoupling the thermal management from the PCB pad design as the package heat sink is situated on the top side of the package. DSC adds a top-side thermal drain to the bottom one providing a superior thermal performance.

3 General acceptance criteria of electronic assemblies



**Figure 11 Schematic of thermal management based on a bottom-side cooling heatsink by an exposed pad.**

**Via-in-pad design**

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-holes in the board called “vias”. The heat is then transferred from the chip over the package die pad and the solder joint to the thermal pad on the board and further through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. A typical hole diameter for thermal vias is 0.2 - 0.5 mm. An array with 1.0 - 1.2 mm pitch can be a reasonable starting point for further design optimization.

Increasing the number of vias does not necessarily translate into a constant decrease of the thermal resistance of the entire assembly setup. Thermal and electrical analysis and/or testing together with a proper board assembly design procedure are recommended to determine the optimal number of vias needed.

The implementation of thermal vias has several impacts on the board assembly as it may require a specific stencil design to avoid the penetration of solder into the via openings. Consequences of such solder wicking would be a decreased stand-off between the PCB and the package, an increased void formation that ultimately could result in an insufficient solder joint area, or surplus solder on the opposite side of the PCB. A first approach for risk reduction should be the prevention of a direct print of solder paste on the via openings. The stencil for such pads is therefore usually segmented in alignment with the via positions (see [Section 4.3, Figure 20](#)).

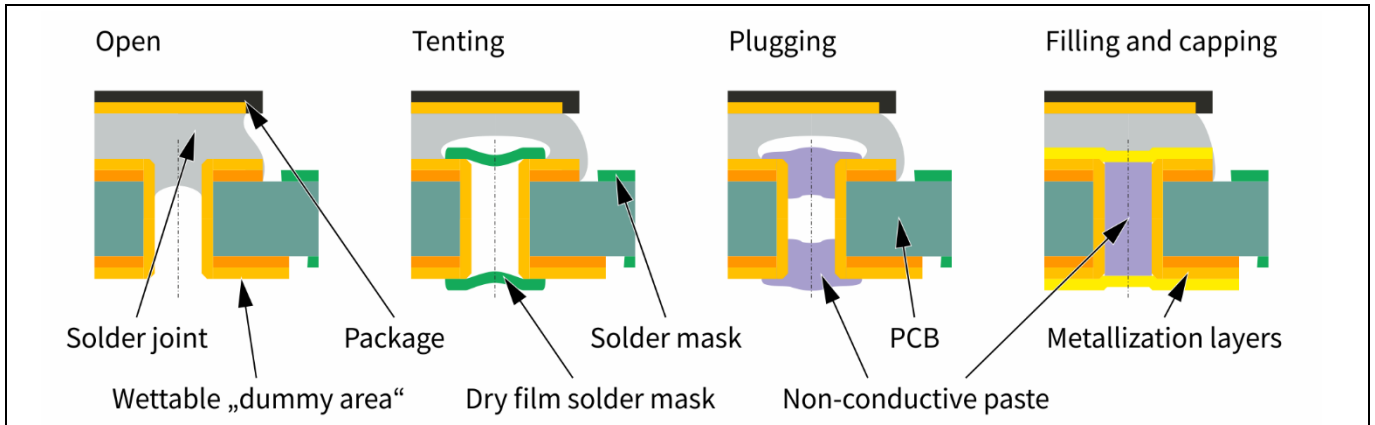
Despite this precautionary stencil design approach the solder may still move into the via, driven by the wetting forces. If the solder then protrudes to the opposite side of the PCB, it may interfere with a second solder paste print process. To minimize the effect, wettable dummy areas surrounding the via opening on the opposite side of the board can catch the surplus solder to avoid beading and solder lumping.

In case the solder variance in volume below the die pad is too high due to the wetting of vias, they can be closed by several techniques. The IPC-4761 describes several types for covering and sealing of vias. They can be generally classified into the three groups of via tenting (simple covering), via plugging (partial filling) and via filling (complete filling). [Figure 12](#) shows several potential solutions for vias-in-pad based on these three classes [19].



**3 General acceptance criteria of electronic assemblies**

In every case, it is recommended to close the via either on the component side or on both sides of the PCB. If it is closed only on the opposite side to the component, the entrapped air is expected to increase the voiding rate significantly. The most advanced method is that of filling the via with a non-conductive paste followed by over-plating. Very small vias (100 µm in diameter or smaller) should be filled with copper and over-plated. In both cases, a planar top side of the pad is important to avoid cavities that will trap gases and form voids during reflow soldering (see Section 3.3).



**Figure 12 Different solutions for via-in-pad design.**

A direct interaction of vias with the assembly process can be avoided by placing them outside the package footprint area. For such an approach, a comprehensive understanding of the overall electrical and thermal concept of the entire application is needed.

For further information about product-specific thermal management of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

**3.3 Solder joint voiding**

Voids in solder joints are primarily caused by flux gases from the organic solder paste compounds that are entrapped in the molten solder during reflow. They may be trapped simply by the balanced inner pressure levels, by geometries (e.g. via-in-pad) or by low wetting regions on the PCB plating (e.g. test probe marks). The parameters on influencing the flux void formation may be as given below.

- Solder paste flux chemistry
- Cleanliness of plated surfaces
- Solder reflow profile
- Paste type (grain size)
- Stencil layout
- Via layout

Solder joints of large heatsinks may tend to increased flux voiding because they do not provide a sufficient ratio between the solder paste volume and the surface necessary for proper outgassing. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment and the electrical use of the component.

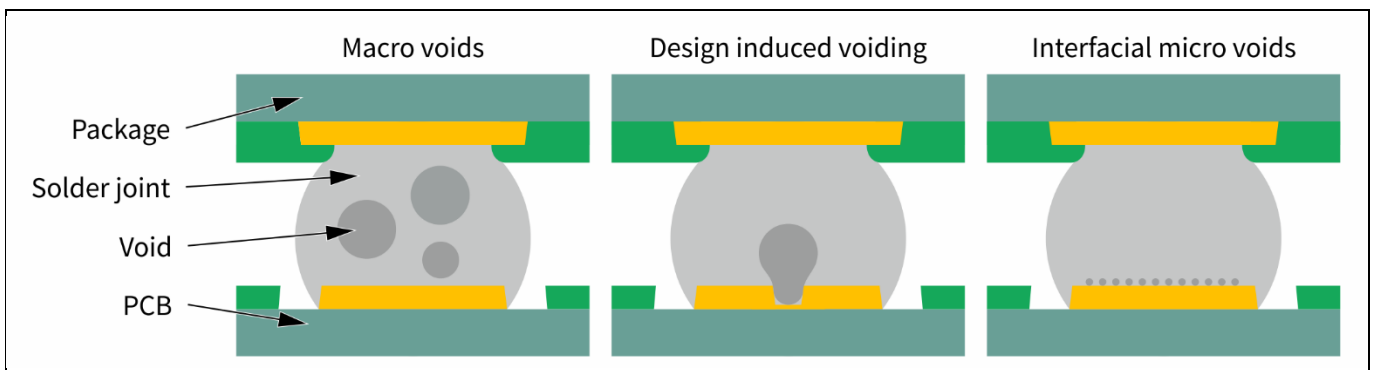
A potential impact of voids on the thermomechanical reliability depends not only on the entire system the board assembly is interacting in but also on the solder void size and location with respect to the pad. The typically larger flux based voids are generally considered to be less critical [21].

3 General acceptance criteria of electronic assemblies

Figure 13 shows a generalized overview of solder voiding which follows the below types.

- Macro voids (“inclusion voids”) are generated by the evolution of flux volatiles during the reflow process when the solder is molten. Sources may be the flux and solder paste or absorbed moisture in laminates. They can be located anywhere within the solder joint and even rise during the time above solder liquidus.
- Design induced void are generated by the presence of micro-vias in the PCB landing pad. Gases are trapped by the via geometry and are therefore located close to it.
- Interfacial micro voids are summarizing multiple types of e.g. small planar micro voids (“champagne voids”) or intermetallic and pinhole micro voids. They typically do not originate from flux residuals but rather from the pad plating itself. They are usually hard to detect by conventional X-ray and typically located close to the solder-to-pad interface.

As multiple factors are influencing the voiding behavior (e.g. flux vs reflow profile) and components are behaving differently (e.g. BGA vs BTC termination) the list of general void reduction strategies for assemblies with a mixed component spectrum is limited.



**Figure 13** Generalized overview of voiding types. From left to right: Flux induced inclusion macro voids, design induced void by micro-via in the pad, interfacial micro voiding.

For further information including typical acceptance levels of voiding, please refer to documents like IPC-7095 or IEC/TR 61191-8 [20][21].

For further information about package specific inspection topics of Infineon devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section. Please also feel free to contact your local sales, application, or quality engineer.

4 Mounting of surface-mount devices

4 Mounting of surface-mount devices

4.1 The SMT process

The I/O terminals of SMD components are located close to the package body. The component placement and solder joint formation are taking place on the surface of the same PCB side. SMD allow for high processing automation and assembly integration. The following factors are generally affecting the quality and reliability of a SMD solder joint.

- PCB design
- Landing pad and stencil layout (“footprint”)
- PCB pad finish (also called metallization or final finish)
- Via layout and technology
- Solder paste formulation
- Solder paste deposition and inspection
- Component placement
- Reflow soldering process, especially the reflow profile

Studies at individual facilities are recommended for board assembly process optimization. The PCB manufacturer’s capabilities, the user’s processes, and the application specific requirements have to be taken into account. Figure 14 shows a typical process flow for single-sided SMD board assembly. The electrical as well as the thermal terminals are located on the same assembly plane that usually eludes assembly steps that include the mounting of additional heat sinks.

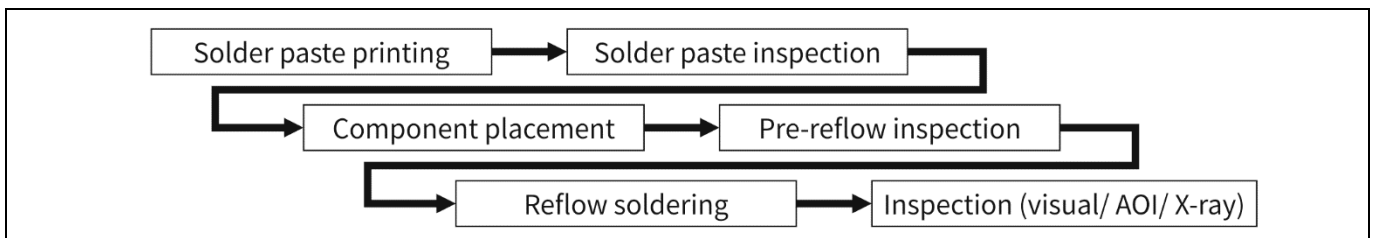


Figure 14 Typical process flow for single-side mounting of SMD.

4.2 Landing pad types and designs

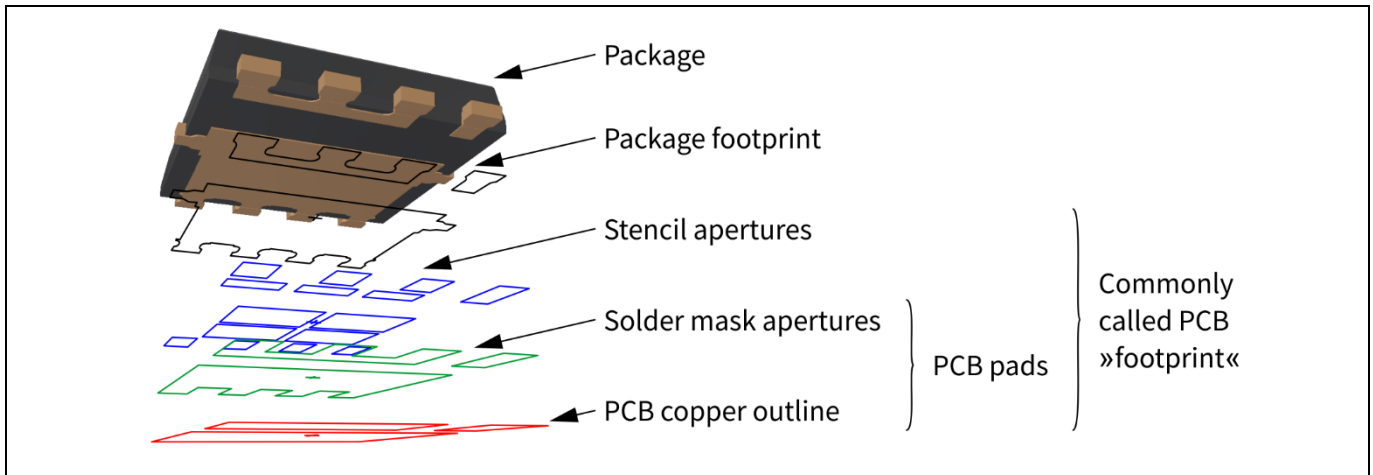
The “footprint” addresses the set of PCB landing pad and stencil design that is needed to reliably connect a SMD by surface mount technology. Infineon footprint recommendations usually consist of the PCB copper outlines, the solder mask apertures and the stencil apertures. These outlines are two-dimensional representatives of three-dimensional technologies. Usually, the footprint design cannot be derived directly by projecting the wettable area of the package terminations to the PCB plane. There should rather be considerations on the specific PCB design, the stencil printing capability, inspection requirements, and the solder joint reliability taken into account. The PCB landing pads usually should be slightly larger than the package terminations but not offset. A mismatched landing pad design can lead to the following issues.

- Swimming/ skewing (package moves in parallel to the PCB plane during reflow soldering) and/or tilt and even tombstoning (package lifts off during reflow soldering)
- Electrical opens or shorts
- Decreased reliability

## 4 Mounting of surface-mount devices

Important parameters of the PCB landing pad include their size and registration type, the thermal and electrical connection concept, copper track minimum lines and spaces, the via design, and the board finish.

Figure 15 shows the concept of a footprint for surface mount technology of electronic devices.



**Figure 15** The “footprint” as a set of PCB landing pad and stencil design.

Documents like the IPC-7351 provide generic requirements and design rules for PCB pad footprints but may also not keep up with latest package designs, electronic assembly requirements (such as densities), and board mount experiences [20]. Infineon therefore provides package-specific pad and stencil designs that are based on in-house studies and experiences. Further package platform specific design and assembly process guidelines may be found in the documents IPC-7093 for bottom-terminated components (BTC) or IPC-7095 for BGA packages [22][23].

*Note:* The footprints that are provided by Infineon are based on experience or generic use cases. It is recommended to consider them as a basis for further application specific studies of electronic assemblers.

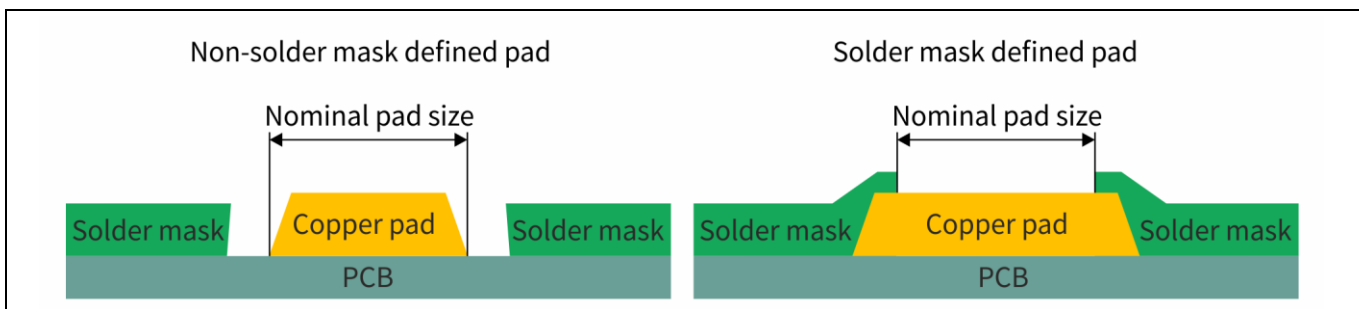
### Pad definition and solder mask layer

The solder mask layer is intended to protect the open copper tracks of a PCB from oxidation. A solder mask dam between electrically separated pads may also reduce the risk of solder bridging. Solder mask dams are also occasionally used to divide larger copper areas into smaller wettable areas. When choosing such an approach it must be considered, that the dimensional and alignment tolerances of the PCB copper layer and solder mask layer structuring can differ significantly. There are generally two basic approaches to define the wettable area of a landing pad as shown in Figure 16.

- Non-solder mask defined pad (NSMD): The wettable area is defined by the copper pad outline („copper defined“). The solder mask surrounds the pad with a certain distance. Dimensions and tolerances of that solder mask clearance have to be specified to ensure that the mask does not partially overlap with the solder pad. Depending on the PCB manufacturer’s tolerances, 50 to 75 µm are widely used. Further downscaling, however, is already requiring for smaller clearance values. The NSMD type is recommended especially for smaller solder pads, due to the increased pad definition accuracy. The sidewalls of an NSMD pad are also wettable which can have an impact on the solder joint geometry and even reliability.
- Solder mask defined pad (SMD): The wettable area is defined by the solder mask aperture outline as the copper pad is extended below the mask. That allows for connecting with large copper areas that is especially beneficial for applications that involve high power conduction. When choosing the SMD type

#### 4 Mounting of surface-mount devices

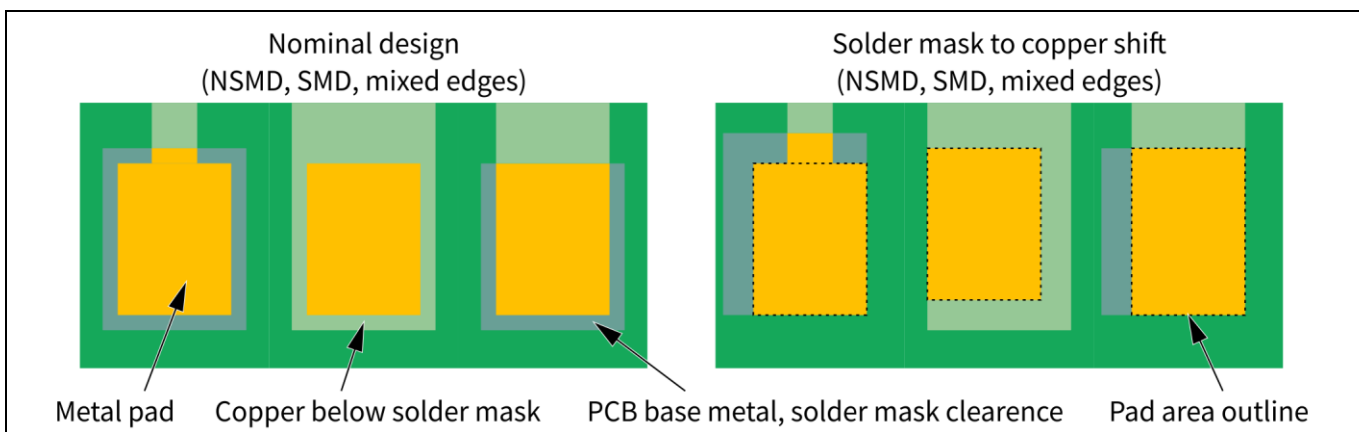
pads, the additional distance between the solder mask top side and PCB landing area should be considered especially with very small packages.



**Figure 16** Concepts of copper defined NSMD and solder mask defined SMD pad design.

*Note:* Mixing both pad definition types in one footprint is not recommended due to the typically high alignment tolerances between the solder mask and the copper layer.

Figure 17 shows the impact of a solder mask to copper shift on a NSMD, SMD and mixed edge design. The position and size of the the wettable area is different with every design. It is therefore not recommended to mix different pad types in one footprint.



**Figure 17** Impact of a solder mask to copper shift on different landing pad designs. A dotted line marks the position and size of the wettable area.

For further details about specific pad and stencil recommendations of Infineon devices, please refer to the package database that is available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show an example of the stencil aperture layout for each package.

### 4.3 Solder paste stencil print

Stencil printing is the most common deposition technique for SMT of electronic devices in terms of precision and efficiency. Alternatives such as screen printing or dispensing are usually used only for special applications.

#### Solder paste composition

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste.

## 4 Mounting of surface-mount devices

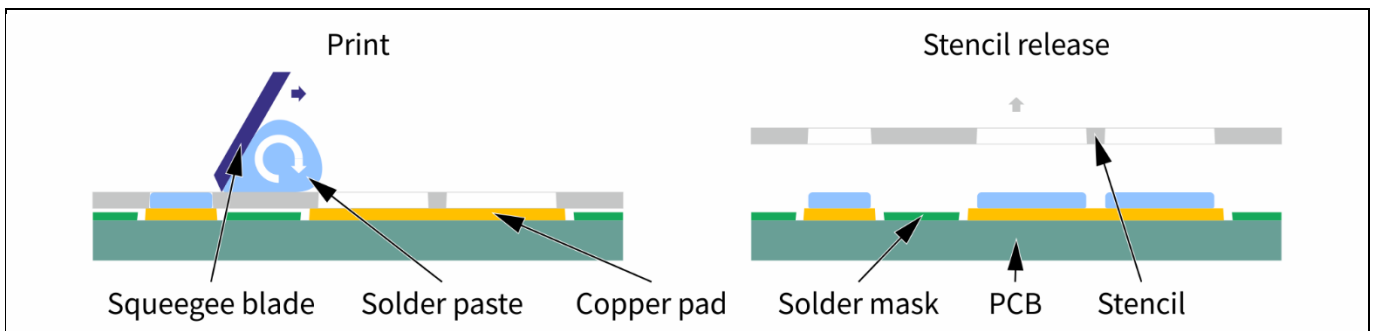
The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides from the surface. The use of a no-clean flux system is generally recommended as flux residuals will remain on the outside of the solder joint after reflow.

The solder paste should be selected based on the requirements and components of the application assembly. The paste composition affects the voiding tendency (evaporation of solvents during reflow) as well as the paste viscosity and therefore the printing performance. This is especially important for fine-pitch components or high-speed printing.

*Note: Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.*

### Solder paste print

During stencil printing the metal stencil sheet is pressed against the PCB pads with a slightly negative lift-off. The solder paste is then rolled over the apertures in the sheet that match the positions of the PCB pads. As the squeegee blade passes the aperture, a part of the solder is rolled into it. The solder paste volume is defined by the stencil aperture size and the stencil thickness. When the stencil is released from the PCB, the amount of solder paste that remains on the pad defines the transfer efficiency. The general process is shown in [Figure 18](#).



**Figure 18 Schematic depiction of solder paste stencil print.**

As a stencil material, laser-cut stainless steel sheets are preferred. Some applications may also require electroformed nickel stencils. Typical thicknesses range between 80  $\mu\text{m}$  (approx. 3 mil) to 150  $\mu\text{m}$  (approx. 6 mil). Sub-miniature packages on the one and large packages on the other hand may also require thicknesses of 60  $\mu\text{m}$  (approx. 2.5 mil) or 200  $\mu\text{m}$  (approx. 8 mil) respectively.

In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. Stepped stencils with multiple thicknesses are usually considered to be a cost-adder. The IPC-7525 may be consulted for further guidance on printing stencil design [24].

The average solder sphere diameter of the alloy powder is specified with the solder paste “Type” as given by the J-STD-005 (see [Table 2](#)) [25]. Typically, Type 4 pastes are used although Type 3 is still applied. The trend, however, goes towards higher types and therefore smaller powder grain sizes. Using a Type 4 paste from pitch 0.4 mm and below might be reasonable approach depending on the specific pad and therefore stencil aperture dimensions. In every case, the following stencil transfer efficiency rules must be respected.

The minimum volume that can be printed by a stencil design with sufficient transfer efficiency depends on the stencil aperture size, stencil thickness, the solder paste type and the stencil aperture wall surface. Generally, the smaller the aperture size of the stencil gets, the lower the maximum applicable stencil thickness becomes.

Solder paste transfer rules describe the efficiency of a printing process to provide a solder volume that is as close as possible to the nominal one. Furthermore, only specific solder paste types (powder grain sizes) can be

**4 Mounting of surface-mount devices**

printed with specific stencil apertures (width/ length, stencil thickness). Figure 19 shows a schematic on the most important stencil transfer rules.

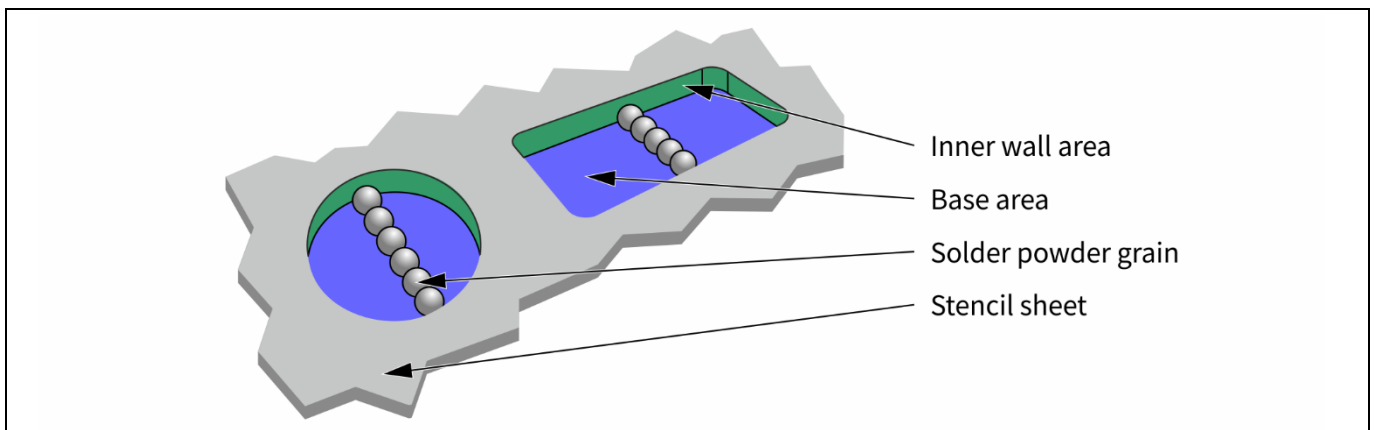
- Sphere rule: The stencil aperture must be filled properly when the squeegee is passing it. The sphere rule refers to the solder paste alloy grain diameter and how many of them could be lined up in the smallest side of a stencil aperture. Rectangular apertures should hold 5, while equilateral ones should hold up to 6 sphere diameters.

$$\text{smallest aperture dimension} \geq 5 \cdot \text{max. grain diameter}$$

$$\text{aperture diameter} \geq 6 \cdot \text{max. grain diameter}$$

- Area ratio: Adhesion forces between the solder paste and the stencil wall are counteracting the adhesion forces between the solder paste and the PCB pad. If the stencil wall area becomes too large (by stencil thickness) in relation to the base area (by stencil aperture size), a considerable solder paste volume may stick to the stencil during its release from the PCB pad. The most commonly applied area ratio feasibility factor is 0.66. That value also considers the typical stencil wall adhesion properties. Surface treatments such as liquid repellent coatings may decrease the feasibility factor or generally stabilize the print volume results.

$$\text{area ratio} = \text{aperture base area} / \text{aperture wall area} > 0.66$$



**Figure 19 Rules of “spheres per length” for rectangular (left) and circular stencil apertures (right).**

Critical designs, which are close to the above-mentioned rules, should be verified by additional design guidelines such as the aspect ratio, which compares the smallest aperture dimension to the stencil thickness. Stencil thicknesses < 60 μm may also be relevant to an examination based on the height equation. It checks if two layers of solder paste grains fit the aperture height.

The shape of the stencil aperture geometry can have a significant impact on the final solder volume irrespective of the actual area ratio or sphere rule compliance. Introducing a certain corner rounding to the stencil apertures are frequently reported to be beneficial to the transfer efficiency (approx. 2 to 2.5 times of the maximums solder paste grain diameter). The objective of rounding the corners is to avoid solder paste from sticking in them when releasing the stencil from the pad but they also have an impact on the area ratio.

Apertures with dimensions ≥ 5 mm might be prone to the scoop-out effect depending on the squeegee stiffness. The blade may sink in, while passing the aperture. Such apertures are therefore usually segmented to provide additional mechanical support to the squeegee.

*Note: Solder paste stencil transfer rules must be respected. A capable and stable board assembly process relies, however, on application-specific experiments.*

4 Mounting of surface-mount devices

**Table 2** Excerpt of the solder powder type classification by weight according to J-STD-005 [25]

Type	80% min. between	10% max. between
1	75-150	150-160
2	45-75	75-80
3	25-45	45-60
4	20-38	38-50
5	15-25	25-40
6	5-15	15-25
7	2-11	11-15

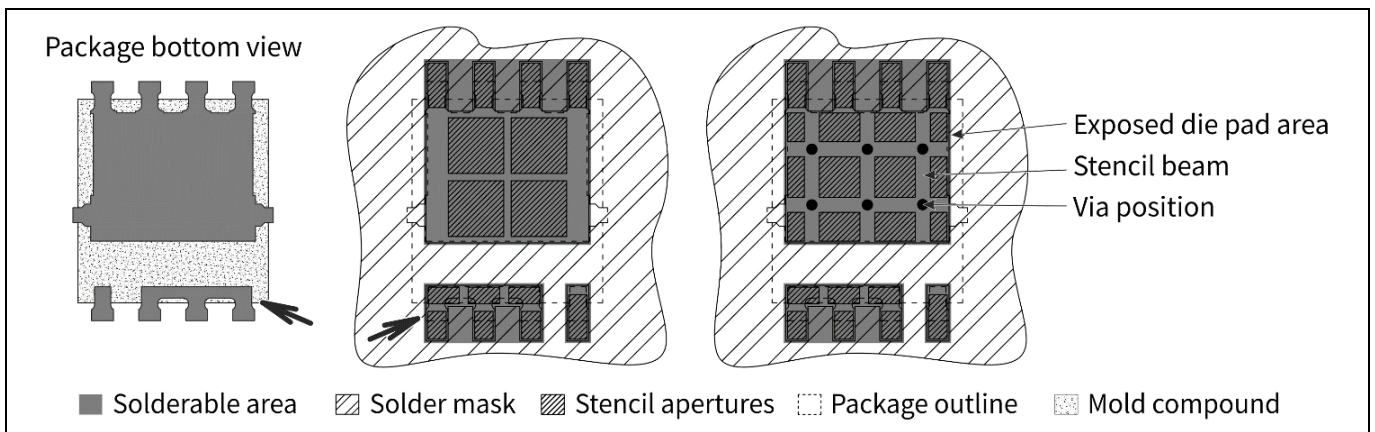
**Solder paste inspection**

A capable and stable solder past print is a critical contributor to the overall board assembly using SMT. Automatic solder paste inspection (SPI) systems are frequently used for inspecting and controlling the printed solder paste depots. They either are built into the printer or are separate modules in an assembly line. Such vision systems can measure for example the solder paste planar coverage or the deposited solder paste volume. Adequate acceptance criteria have to be defined individually.

**Stencil and landing pad design**

Neither the copper pad nor the stencil aperture cross-sections feature perfectly rectangular structures. Depending on the board manufacturing technology, the initial copper cladding and final pad thickness, the steep line edges can vary. The stencil outline should seal the PCB pad also when considering all process and material tolerances. A reduction of the stencil aperture is therefore recommended especially for small pad sizes. The following guidelines should be considered when going into the PCB pad design. Relevant examples are shown in [Figure 20](#).

- SMD vs NSMD pads may produce different wettable area sizes
- L-shape prints are not allowed as the passing squeegee can bend up the resulting edge
- Prints on large pads should be reduced sufficiently to avoid component swimming, tilting, tombstoning or solder beading
- Large prints e.g. for heat sink pads should be segmented to avoid scooping
- The stencil beams from print segmentation may be used to cover openings of vias-in-pad (see [Section 3.2](#))



**Figure 20** Examples of stencil print segmentation. The print for fused pads should be segmented in order to avoid L-shaped apertures (left and center). When having vias-in-pad it is beneficial to use the stencil beams to cover the via openings (center and right).



## 4 Mounting of surface-mount devices

Infineon stencil design recommendations are usually applicable to a certain range of sheet thickness as long as the general stencil printing rules are respected. Some designs may be based on specific solder volumes. In such a case, the relevant stencil thickness is given in the pad and stencil design.

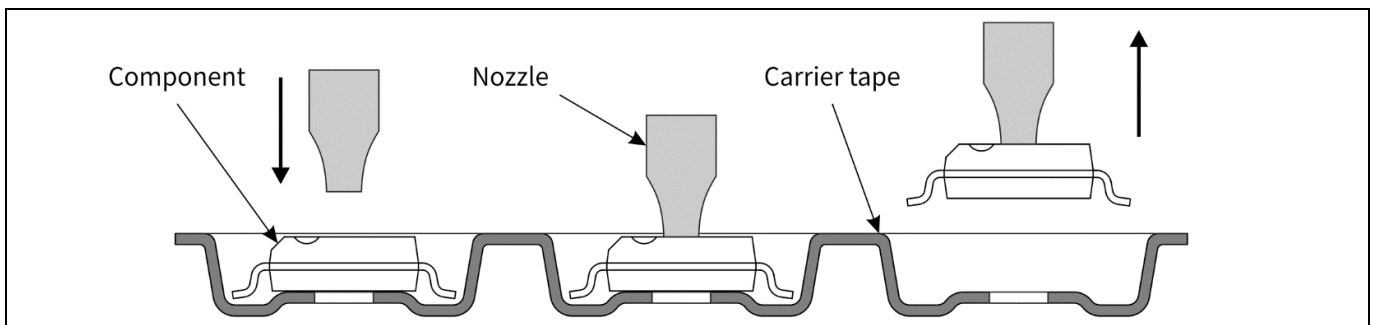
For individual design adaptations especially on reaching the optimum amount of solder, the stencil thickness, the PCB pad finish, quality and solder masking, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

For further details about specific pad and stencil recommendations of Infineon devices, please refer to the package database that is available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show an example of the stencil aperture layout for each package.

### 4.4 Component placement of SMD

The SMD components have to be placed accurately onto the solder paste depot on the PCB. Automated placement machines are commonly used to reach placement accuracies of approx.  $\pm 50 \mu\text{m}$ . Manual placement might be possible depending on the package size and pitch but is generally not recommended. The automated machines can work according to different principles like pick-and-place or collect-and-place. Vacuum nozzles or mechanical grippers may be used for moving the components (see [Figure 21](#)).

Integrated vision systems are inspecting the component as well as alignment markings on the PCB before placing the components to their programmed positions. Fiducials of different geometries are commonly used for aligning the PCB. They are either located at the edge of the board or additionally placed to individual mounting positions (so called “local fiducials”).



**Figure 21** Component pick-up sequence from carrier tape using a vacuum nozzle in contact mode.

High volume automated placement machines are usually fed from standardized tape & reel, tube or tray packing (see [Section 2.4](#)).

Although the self-alignment effect caused by the solder surface tension will support the formation of a reliable solder joint the maximum displacement should not exceed approx. 20% of the PCB pad width. The following guidelines should be considered for component placement.

- The alignment on large boards should be supported by local fiducials to compensate for PCB tolerances such as shrink.
- The component inspection by the placement vision system should be adapted to the relevant package type. The alignment by lead identification might be preferred for leaded and leadless terminations while the alignment by package outline might be used for pre-balled components.
- The placement forces provided by automated placement machine vendors are usually applicable to a wide range of SMD package types. Increasing placement forces may lead to solder squeezing and ultimately to solder joint shorts. Reduced placement forces may lead to insufficient contact between the component and the solder paste. This may result in shifted or dropped components in the following process steps.

**4 Mounting of surface-mount devices**

- A pick-up nozzle that is suitable for the component body size should be used. The nozzle should be slightly smaller than the component body. While a nozzle, that is too wide, may suck in air. A nozzle, that is too small, may not create the necessary force to avoid component shifts during the movement of the picking head. Irregular package body surfaces might be more suited to be picked by mechanical grippers.

For further information about placement of Infineon devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section. Please also feel free to contact your local sales, application, or quality engineer.

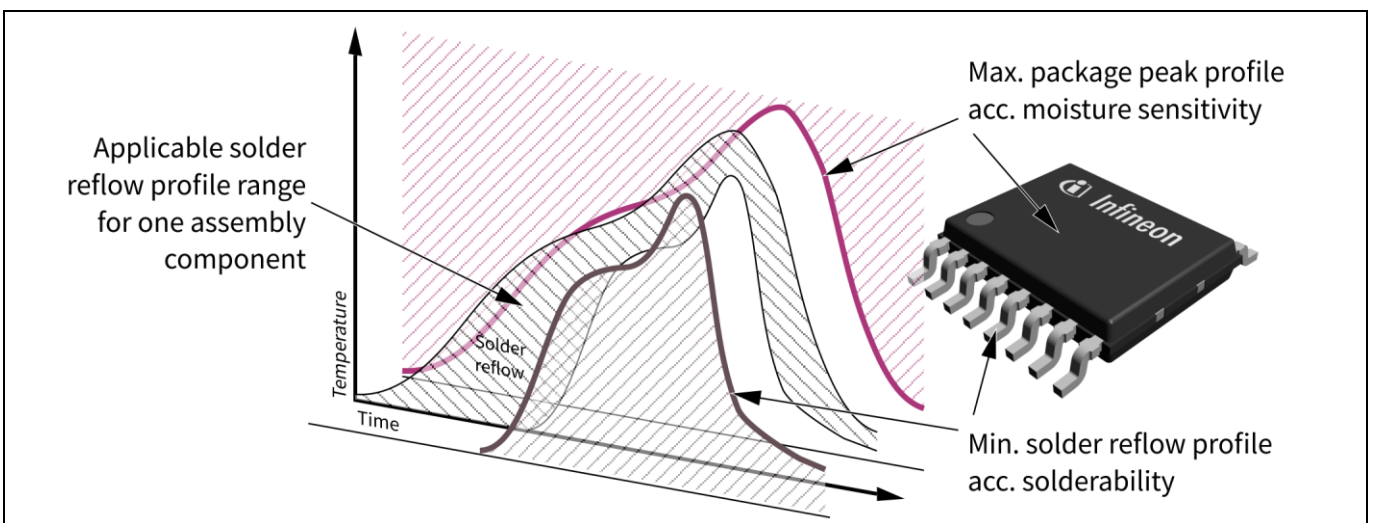
**4.5 Reflow soldering**

Reflow soldering in a forced convection reflow oven is the most common technique to form a mechanical, electrical and thermal connection between the SMD components and the PCB. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

By melting the metallic powder particles in the solder paste, the metal pads of the component and the board are joined together while creating a strong metallurgical bond after re-solidification of the solder. During the reflow process, each solder joint has to be exposed to temperatures above the melting point of the solder (i.e. liquidus of the solder alloy) for a sufficient time. The package body peak temperature shall thereby not exceed the maximum allowed value.

Reflow profiles for board assembly should be developed based on specific process needs and board designs. The temperatures and durations experienced by the SMD package bodies shall thereby not exceed those from the respective J-STD-020 moisture sensitivity classification (see Section 2.2) [7]. The minimum temperatures and durations at the SMD terminations shall not come below the requirements for proper solder wetting (see Section 2.3). Figure 22 shows a schematic of a solder reflow profile at the termination of one assembly component and its boundaries. As an example, the maximum temperature experienced by the component should stay below the maximum package peak temperatures and above the minimum reflow peak temperatures at its terminations.

*Note: The upper reflow processing boundary of a SMD i.e. the maximum package body peak temperature, is determined by classification profiles that must not be confused with the actual reflow soldering profile that has to be applied in the board assembly.*



**Figure 22 Relation of solder reflow profile range to its boundaries. These are given by the highest package peak and the lowest reflow peak temperatures and durations.**

## 4 Mounting of surface-mount devices

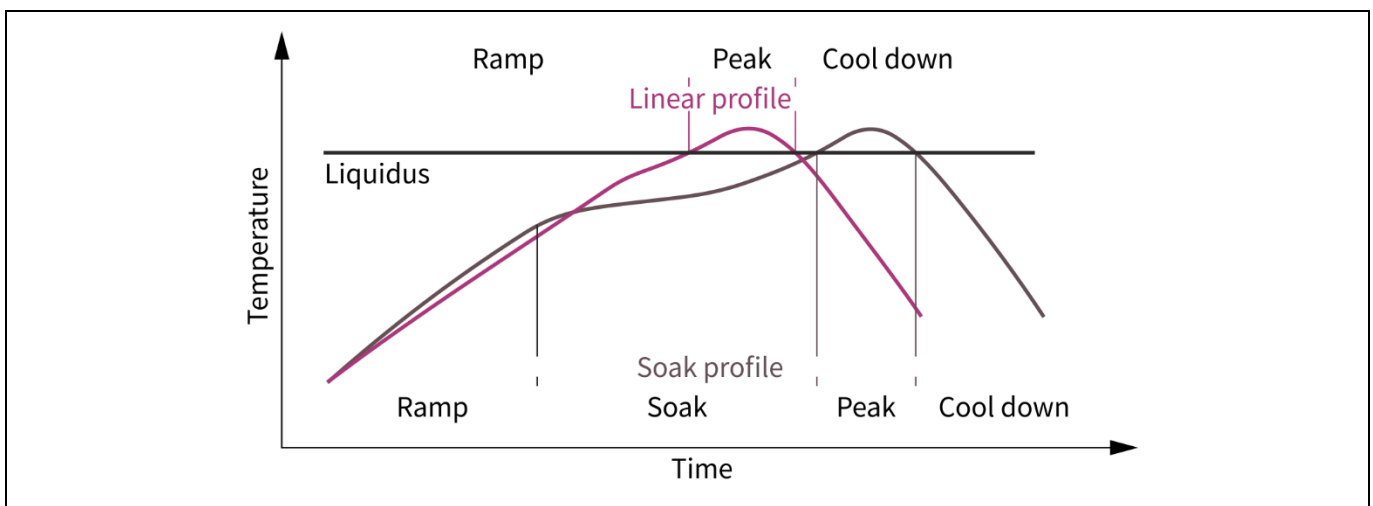
Typical PCB assemblies contain various components of different types and sizes. The reflow settings therefore have to match the allowed profile range of all the components at their package bodies and terminations respectively. Components with large thermal masses do not heat up as readily as lightweight components. In addition, the position and the surrounding of the component on the PCB, as well as the PCB thickness, have a significant impact on the solder joint temperature. It is therefore recommended to measure the temperatures at critical positions on the PCB. The optimum reflow profile of a board assembly is governed by several parameters.

- Board thickness and layout
- Differences in thermal mass of all components
- Maximum allowed package body peak temperature of the most sensitive components
- Recommended reflow profile for the solder paste
- Oven design and number of zones
- Convection flow rate

*Note: The solder reflow profile sections do not coincide with the oven heating zones due to temperature transfer efficiency and heating delay by the thermal masses.*

A soldering profile can be divided in four processing zones: ramp-up, preheating (soak), reflow peak, and cool down. Usually the profile type is chosen between the linear and the soak concept as shown in Figure 23. While the linear type directly ramps to the reflow peak, the soak type stays at a certain pre-heating temperature in the range of approx. 150°C – 180°C for 60 s – 90 s in order to equalize the temperatures of all components. The termination temperature might experience around 60 s of “time above liquidus” (TAL) that is of approx. 220°C when using SAC305 solder alloy. The peak temperature at the termination may vary in the range of > 235°C to < 260°C depending on the minimum solder reflow peak temperatures and the allowed maximum package body peak temperatures of each assembly component [28].

The different reflow profile types can result in different qualities of solder voiding and spatter tendency depending on solder paste flux and package type but can also impact the production cycle time.



**Figure 23 Qualitative depiction of reflow options using a linear (ramp to peak) or a soak (ramp to soak to peak) profile.**

Reference reflow profiles for soldering application are given by the solder paste manufacturers. They are usually providing a suitable starting point for further optimization. General requirements for electronic-grade

## 4 Mounting of surface-mount devices

solder alloys and fluxes can be found in the standards J-STD-001 and J-STD-006 [17][26]. Further support on reflow profiling might be found in the IPC-7530 or IEC/TR IEC 60068-3-12 [27][28].

### Minimum reflow conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the wettability qualification. The solderability of the terminations of Infineon components is tested according to the standards J-STD-002 or IEC 60068-2-58 [11][12].

### Maximum reflow conditions and cycles

Components that are moisture-sensitivity level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states the MSL as well as the maximum reflow temperature according to the J-STD-020 [7].

### Double-sided assemblies

Typical Infineon SMD products are generally suited for double-sided PCB assemblies. The following guidelines should be considered.

- Components on the first PCB side will experience an additional reflow step. Products that are MSL classified can be reflowed three times.
- The components on the first PCB side are held in place only by the solder wetting forces during the second reflow step. Gravity acting at the solder joint will elongate them. This shape will be frozen during cooling and therefore will result in a higher stand-off on that board side.
- Heavy components should be mounted during the second run of a double-side assembly. In case such a procedure is not applicable, the use of an appropriate SMD adhesive might be considered.
- If the maximum floor time per MSL classification of already mounted components is expected to be exceeded during the first and second reflow run, suitable measures to avoid moisture soaking have to be applied. Such measures might be storage in moisture-barrier bags or in a dry cabinet or a dry bake of the entire PCB prior to second reflow.

### Alternative heating concepts

The most frequently used reflow ovens used in mass production work with forced convection. The heating concept is based on blowing hot air or nitrogen at different temperatures in different zones onto a board assembly. The boards travel through these zones on a conveyor band.

Alternative reflow oven concepts are based on heat transfer by infrared (IR) or vapor phase.

During infrared soldering, the components are heated by the absorption of IR radiation. The temperature of the various components may vary severely since the radiation absorption mostly depends on the material and the IR wavelength, and less on the radiator temperature. As the metallic terminals feature a low absorption rate and reflect the radiation, the heat has to be supplied to the solder joints through the components, the board, and the heated ambient air. The solder joint temperature may therefore not correlate directly with the thermal masses of the components but additionally with their radiation absorption, the temperature of the PCB and that of the surrounding air. Compliance with the upper and lower processing boundaries of the SMD should therefore be ensured by specific temperature measurements at critical positions.

The vapor phase soldering technology provides the least risk of overheating because it can limit the temperature by the active fluid itself. The vapor temperature may be chosen to be slightly above the melting point of the solder alloy. The atmosphere in a vapor phase oven is usually free from oxygen. Vapor phase ovens

## 4 Mounting of surface-mount devices

typically feature one process chamber and are not conveyor-driven. They are therefore usually not used for in-line mass production but are implemented for batch processing.

For further information about SMD reflow and reflow sensitivity of Infineon devices, please refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

### 4.6 Wave soldering of SMD

SMD are generally not designed to withstand a wave soldering process in which the whole package body is getting in contact with the molten solder.

In case SMD are considered for mounting by wave soldering, e.g. in a mixed THD/SMD assembly, the resistance of the product against thermal shock according to JESD22-A111 should be confirmed upfront [29].

The PCB pad design for SMT mounting cannot be applied and a suitable version for the wave soldering must be designed. Furthermore, the application of an appropriate SMD adhesive prior to the soldering should be considered. In every case, individual investigations on a per-product basis are necessary.

### 4.7 Inspection of mounted SMD

Automated post-reflow inspection is usually implemented in-line and covers a variety of objectives on board assembly quality such as below.

- Component presence/absence, offset, polarity, “billboarding”/ ”tombstoning”, ...
- Excessive/insufficient solder volume, solder bridging/opens, non-wetting, voiding, ...

Optical inspections may already be applied pre-reflow after component placement. Assemblies with severely misplaced or wrongly chosen components can then already be sorted out. The general acceptance criteria of electronic assemblies according to IPC-A-610 should be considered [16].

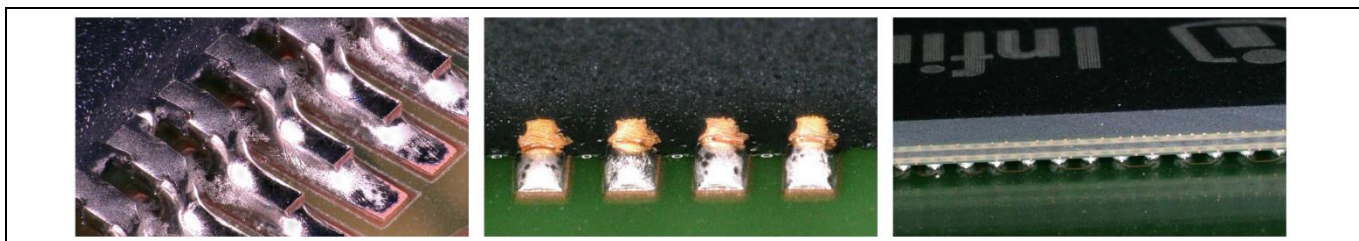
Production-relevant inspection techniques shall be of a non-destructive nature. That does also include methods that involve X-ray radiation (see [Section 2.6](#)). For engineering tasks, cross sectioning can offer detailed information about the solder joint quality. The method provides valuable information about the solder joint quality during the design process of new products. Due to its destructive character, cross sectioning during monitoring is naturally not practical.

#### Visual inspection

A visual inspection of the solder joints can be done using an optical macroscopes and/or microscope. In-line visual inspection of board assemblies is usually covered by machines with conventional 2D or with 3D automated optical inspection (AOI). They are working with different lighting that is specialized to multiple test objectives. That can be for example pin 1 orientation or solder joint bridging control.

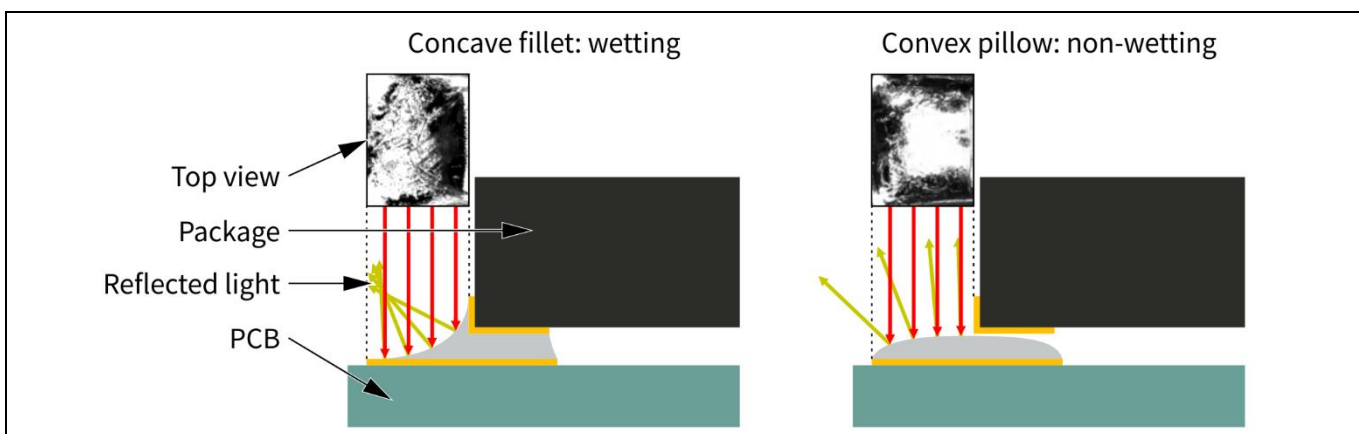
The application of AOI for controlling the solder joints of outer e.g. gullwing-shaped terminations is a standard procedure. The solder joints of leadless BTC are mainly formed underneath the package. Consequently, a reliable visual inspection of such solder joints using AOI is limited. Optional wettable flanks for so called “lead tip inspection” (LTI) enable the optical inspection of such leadless components as an integral package feature. A visual inspection of bottom-only BGA or LGA solder joints with conventional AOI systems is not possible. Even a side-view can only reveal a certain number of the solder joints as can be seen in [Figure 24](#).

4 Mounting of surface-mount devices



**Figure 24** Photographs of SMD solder joint examples with (from left to right) gullwing leads, leadless terminations, and solder balls. The terminations may inherently allow for optical inspection, must be supported by additional wetting features or are not feasible as the solder joint is only formed underneath the package body.

The LTI features allow the optical inspection of leadless termination types. The wettable flank of the LTI feature on the termination provides information about the solder wetting of the termination landing area below the component. Usually, the reflection pattern of a concave solder fillet is considered pass and of a convex solder pillow/bead is considered to be fail as shown in Figure 25. The reproducible formation of an optically inspectable solder joint LTI fillet requires good wetting and a stable position of the entire joint during reflow.



**Figure 25** Concept of the wettable flank of an LTI feature for optical inspection of leadless packages.

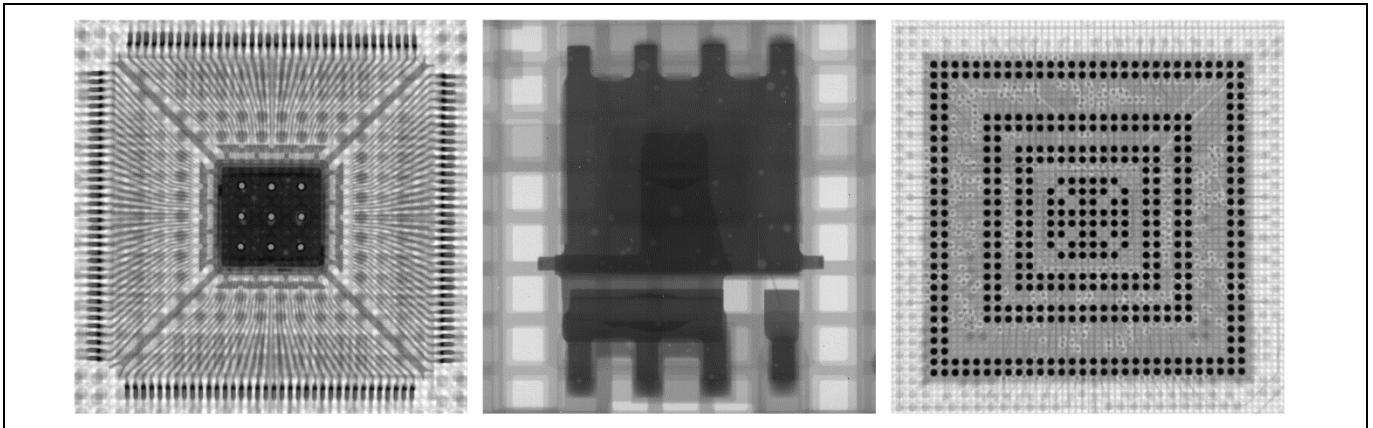
**X-ray inspection**

Automated X-ray inspection systems are appropriate for efficient in-line control of components that cannot be inspected properly by optical systems. That covers for examples exposed pads or solder joints of bottom-only terminations. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transfer routines. These systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. Some defects such as broken solder joints are not easily detectable by X-ray.

Figure 26 shows typical X-ray photographs of a gullwing QFP, leadless SON and pre-balled BGA component that is mounted on board. The X-ray reveals the different solder joints as well as further package features such as the lead frame, wire bonds or redistribution layers. Outer and inner metallization layers as well as vias can be seen in the PCB.

Semiconductor devices may be sensitive to excessive X-ray radiation. Please therefore refer to Section 2.6.

4 Mounting of surface-mount devices



**Figure 26** X-ray photographs of SMD solder joint examples with (from left to right) gullwing leads, leadless terminations, and solder balls. The X-ray reveals different features of the component, the PCB and the interconnect.

5 Mounting of through-hole devices

5 Mounting of through-hole devices

5.1 The THT process

The I/O terminals of THD components are forming long leads. The component placement and solder joint formation are taking place on different sides of the PCB. THD involves semi-automated to manual process steps and allows the manufacturing of high power assemblies. The following factors are generally affecting the quality and reliability of a THD solder joint.

- PCB design and holes for soldering
- Component insertion
- Heat sink mounting concept
- Soldering method (especially the type of wave)

Studies at individual facilities are recommended for board assembly process optimization. The PCB manufacturer’s capabilities, the customer’s processes, and the application specific requirements have to be taken into account. Figure 27 shows an exemplarily process flow for THD board assembly. Through-hole packaged parts are mostly supplied with the leads projecting straight out of the mold body. The components are mounted by inserting their leads into plated through-holes in the PCB. Many practical power circuits use additional heat sinks that are mounted to the device tabs to enhance thermal performance.

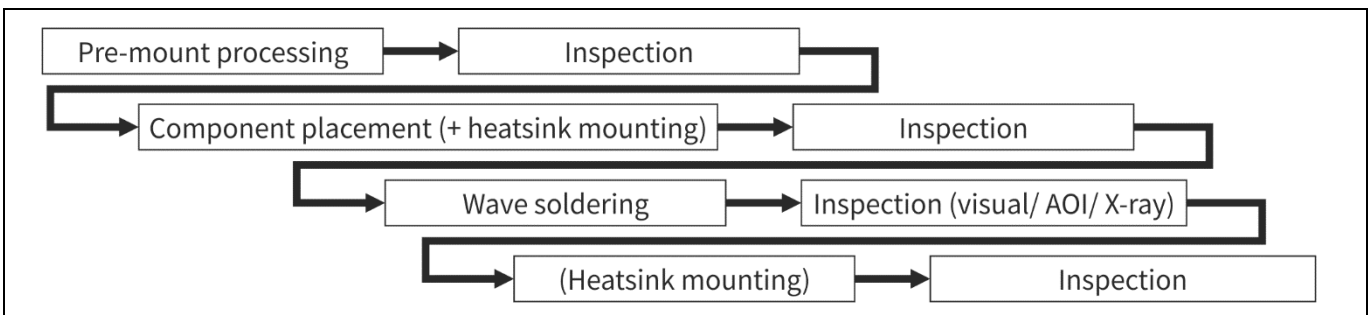


Figure 27 Typical process flow for single-side mounting of THD.

5.2 Pre-mounting processes and mounting materials

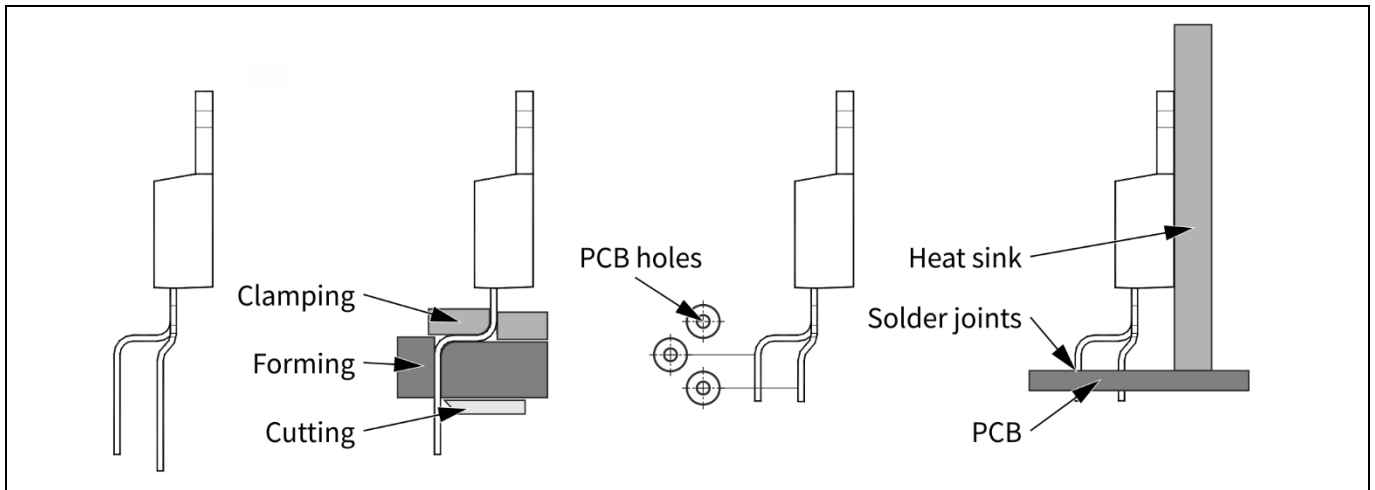
The through-hole devices are inserted into drilled and metallized holes in the circuit board. It is therefore common to change the lead length and direction prior to the insertion in order to fit the pitch of the solder holes. The mounting of additional external heat sinks may also require the reconfiguration of the straight leads. Figure 28 shows application cases for lead bending. The pre-mounting process usually involves the following items.

- Lead clamping
- Lead cutting
- Lead bending

Clamping, bending and cutting are usually executed sequentially and maybe using only one tool. During the procedure focus should be set on not to harm the package body especially at the point, where leads protrude it. Manual bending and cutting is generally not recommended.



5 Mounting of through-hole devices



**Figure 28 Overview on THD pre-mounting steps. The lead clamping, forming, and cutting may be executed with one tool. Lead bending may be executed for mounting hole offset compensation or heatsink arrangement.**

For further information about pre-mounting of Infineon through-hole devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section. As this topic is also specific to the product, you may also refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

**5.3 Component placement of THD**

THD are inserted to the plated through-holes either with special automatic equipment or manually. During this insertion, special care has to be taken that excessive deformation or violent bending is avoided. The diameter of the drill holes in the PCB have to be appropriate for the tolerances of component leads, drill hole position placement accuracy, and properties of the solder alloy used.

**5.4 Heat sink mounting**

For special packages with high power dissipation, heat sinks can be mounted before or after soldering the leads. Screw mounting is a traditional assembly method using a screw, nut, and washer. The clip mounting method has become popular because it is simple and reliable. The process is fast and appropriate for mass production assembly. The screw mounting is applied at one end of the package during fastening and can cause uneven contact pressure and bad thermal contact, whereas the clip is mounted on the package center and therefore results in more uniform contact pressure. If screw mounting is used, the following items should be considered.

- Heat sink design (incl. roughness, flatness)
- Attachment holes and torque for screw mounting
- Insulating material (e.g. washers, spacers)
- Thermal grease
- Mounting torque

Applying the proper mounting torque with screw mounting is the key factor in obtaining an adequate contact pressure along the contact surfaces of the package and the heat sink. Improper and excessive mounting force,

## 5 Mounting of through-hole devices

however, can damage the package and even the device die. The recommended mounting torque should be respected, as higher values do not necessarily contribute to a reduced thermal resistance of the contact area.

Double-sided heat sink mounting is not recommended as high mechanical stresses may occur in case of unsuitable mechanical heat sink properties.

For further information about heat sink mounting of Infineon through-hole devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section. As this topic is also specific to the product, you may also refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

### 5.5 Wave and selective wave soldering

THD components are designed for wave or selective wave soldering. These processes use a tank holding molten solder. The components are inserted into the PCB. The loaded PCB is then passed across a pumped wave or cascade of solder. The solder wets the package leads on the opposite side of the PCB as well as the exposed metallic areas of the board. The body of the package gets heated only by conduction from the leads that are in contact with the solder. As a result, the package body is cooler and the temperature gradient between leads and body and inside the package is steeper compared to reflow soldering.

Various types of wave soldering machines are available. The basic components and operating principles of these machines are the same. A standard wave solder machine has three zones: the fluxing zone, the preheating zone, and the soldering zone. An additional fourth zone for cleaning may be used depending on the type of flux that has been applied. When using Pb-free solder alloys, a nitrogen atmosphere is recommended.

A common method is the dual-wave soldering. The first wave has a turbulent flow and therefore guarantees wetting of nearly all shapes of leads and board pads, but also results in a large number of solder bridges. These solder bridges must then be removed by the second, laminar wave.

Selective soldering is typically used when only a few THD components have to be mounted to a PCB mixed with SMD. Generally, this is done after the other components are already mounted by reflow soldering.

The heat resistance of wave-solderable THD is tested according to JESD22-B106. That provides the maximum acceptable temperature and time for wave soldering [9].

Further information and guidelines for mass soldering processes using wave soldering may be taken from IPC-7530 [27].

### 5.6 Alternative mounting methods

Some applications might use mounting methods that are alternative to the wave soldering. General guidelines should be followed irrespective of the used mounting method.

- The maximum temperature of the package body and leads must not exceed the maximum allowed ones.
- The maximum allowed time at high temperatures must not exceed the maximum allowed ones.
- If heat is applied to the leads, the maximum temperature at the package body must not exceed the maximum allowed ones.

#### Reflow soldering

THD are generally not qualified for reflow soldering as the product experiences the soldering temperature directly at the package. In the following application cases, the product undergoes a reflow profile cycle.

## 5 Mounting of through-hole devices

- Heat sink mounting by reflow soldering: The THD is mounted to the heat sink by solder paste printing, pick-and-place, and reflow soldering.
- Pin-in-paste: Solder paste is printed onto a PCB near or over drill holes through which the leads are then inserted into. The reflow of the solder paste is done together with soldering the surface mount components.

The thermal load to wave-soldered THD focuses on the leads. The die in the package body is therefore experiencing a different temperature than the leads. In contrast, a reflow-soldered THD experiences an entirely different temperature load.

- The temperature is nearly the same for the whole package compared to wave soldering.
- The duration of the peak temperature load to the package is much longer compared to that during wave soldering.

The heat resistance and moisture sensitivity of THD that are reflow soldered have to be tested upfront according to the J-STD-020 standards [7].

### Further mounting techniques

Further mounting techniques for THD include laser welding, resistance welding, and soldering, hot bar soldering, and manual soldering with a soldering iron or hot-air gun. Especially during manual hand soldering it must be considered, that the temperature at the mold body does not exceed the allowed one.

*Note: The applicability of any mounting method other than wave / selective wave soldering is product specific and cannot be derived from a package type.*

## 5.7 Inspection of mounted THD

The proper fill of THD solder joints in the PCB mounting hole are usually assessed based on visual inspections. It may also be assessed using X-ray analysis or cross-sections. While cross-sectioning is a destructive method per-se, the application of X-ray may provide a suitable mass inspection technique if set up properly (see [Section 2.6](#)).

## 6 Cleaning and protection of assemblies

### 6 Cleaning and protection of assemblies

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a SMD component is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process. Especially for power applications, leakage currents and the potential for shorting below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. Please contact the flux and solder-paste manufacturer for recommended cleaning solutions.

Specific devices might be sensitive to certain cleaning methods. That applies for example to packages with open sensor ports that should not be entered by cleaning solutions or air blows. Ultrasonic cleaning might also be harmful to sensor concepts that are sensitive to mechanical impact (i.e. microelectromechanical systems, MEMS).

*Note: Cleaning below SMD package bodies is not likely to be complete; residues may remain.*

Cleaning might be necessary as a preparation for protective coatings, overmold covers and similar approaches. They are used to prevent damage to the assembly by external influences such as mechanical abrasion, vibration, mechanical shock, humidity, hand perspiration, chemicals or corrosive gases. Coatings are supposed to act as electrical isolation and impervious covers that should adhere well to the various circuit board materials. There is a wide variety of different coating technologies, materials and processes.

*Note: Infineon cannot provide general recommendations on protective coatings that cover the broad variety of technologies, materials and processes.*

For recommended cleaning solutions, please contact the solder paste or flux manufacturer. In any case, please take into account the chemical, electrical, mechanical and thermo-mechanical interactions between the coating and the board or the components.

## 7 Single device processing and rework

### 7 Single device processing and rework

Infineon device solder joints are generally reworkable. The reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

When reworking THD components their resistance to solder shock according to JESD22-B106 must be respected [9].

A rework process of SMD packages is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items.

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. The impact of rework tools has, however, to be assessed properly. In general, a higher rate of manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the SMD component according to the J-STD-020 [7]. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the J-STD-033 standard [8]. Please also refer to the recommendations of the PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (e.g. hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further reflow cycle in terms of the J-STD-020 [7]. Internal investigations have shown that the temperature profile should be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to de-solder the component prior to return. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection, Infineon may request that the PCB or part of the PCB with the component still attached should be sent.

*Note: Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (i.e. onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about rework of Infineon devices, please refer to the *Recommendations for board assembly of Infineon packages* documents that are available on the Infineon web page [1]. Please choose a specific package when searching the database, which will then show you the relevant document in the download section. As this topic is also specific to the product, you may also refer to the individual product application note and data sheet documents that are available on the Infineon web page [6]. Please also feel free to contact your local sales, application, or quality engineer.

8 Acronyms and abbreviations

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Ag	.....	silver plating
AOI	.....	automated optical inspection
AXI	.....	automated x-ray inspection
BGA	.....	ball grid array
BPL	.....	barcode product label
BSC	.....	bottom-side cooling
BTC	.....	bottom-terminated component
DSC	.....	double-side cooling
ENEPIG	.....	electroless nickel electroless palladium immersion gold
ENIG	.....	electroless nickel immersion gold
ESD	.....	electrostatic discharge
Gy	.....	Gray; unit of absorbed ionizing radiation dose
HAL	.....	hot air leveling
HASL	.....	hot air solder leveling
HIC	.....	humidity indicator card
IMC	.....	intermetallic compound
I/O	.....	input/output
IR	.....	infrared
LGA	.....	land grid array
LTI	.....	lead tip inspection
MBB	.....	moisture barrier bag
MEMS	.....	microelectromechanical systems
MSL	.....	moisture-sensitivity level
Ni/Au	.....	nickel/gold
NSMD	.....	non-solder mask defined pad
OSP	.....	organic surface/ solderability preservative
PCB	.....	printed circuit board
PTH	.....	plated through hole
QFN	.....	quad-flat no-lead package
Rad	.....	unit of absorbed ionizing radiation dose
RH	.....	room humidity

## 8 Acronyms and abbreviations

SAC	.....	tin silver copper (SnAgCu)
SiP	.....	system-in-package
SMD	.....	solder mask defined
SMD	.....	surface mount device
SMT	.....	surface mount technology
Sn	.....	matte tin plating
SOM	.....	system on module
SPI	.....	solder paste inspection
TAL	.....	time above liquidus
THD	.....	through-hole device
THT	.....	through-hole technology
TO	.....	transistor outline package
TSC	.....	top-side cooling

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## Revision history

### Revision history

Document revision	Date	Description of changes
5.00	2022-09-22	Complete update of document template and structure, review of technical content

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